

GENERAL DESCRIPTION

The SGM61132A is an adaptive constant on-time control (ACOT) synchronous Buck converter with a wide input voltage range of 4.5V to 17V. This device has 3A output current capability and operates at pseudo-fixed frequency. It is an easy-to-use device with power switches and internal compensation circuit, which are all integrated in a small 6-pin package, and supports low equivalent series resistance (ESR) output capacitors. A typical 1ms soft-start ramp is also included to minimize the inrush current.

Protection features include cycle-by-cycle current limit, hiccup mode short-circuit protection and thermal shutdown in case of excessive power dissipation.

The SGM61132A enters in pulse-skip mode to improve efficiency during light load operation.

The SGM61132A is available in a Green SOT-563-6 package.

FEATURES

- Wide 4.5V to 17V Input Voltage Range
- 0.806V to 7V Output Voltage Range
- 3A Continuous Output Current
- Integrated 56mΩ/35mΩ Power MOSFETs
- Shutdown Current: 1μA (TYP)
- 1ms Internal Soft-Start Time
- Pseudo-Fixed 500kHz Switching Frequency
- Adaptive Constant On-Time Mode Control
- Pulse-Skip Mode
- Cycle-by-Cycle Over-Current Limit
- Thermal Shutdown with Auto Recovery
- Available in a Green SOT-563-6 Package

APPLICATIONS

- 12V Distributed Power Supply Buses
- Industrial and Consumer Applications
- White Goods
- Surveillance
- Set-Top Boxes
- General Purpose Point of Load

TYPICAL APPLICATION

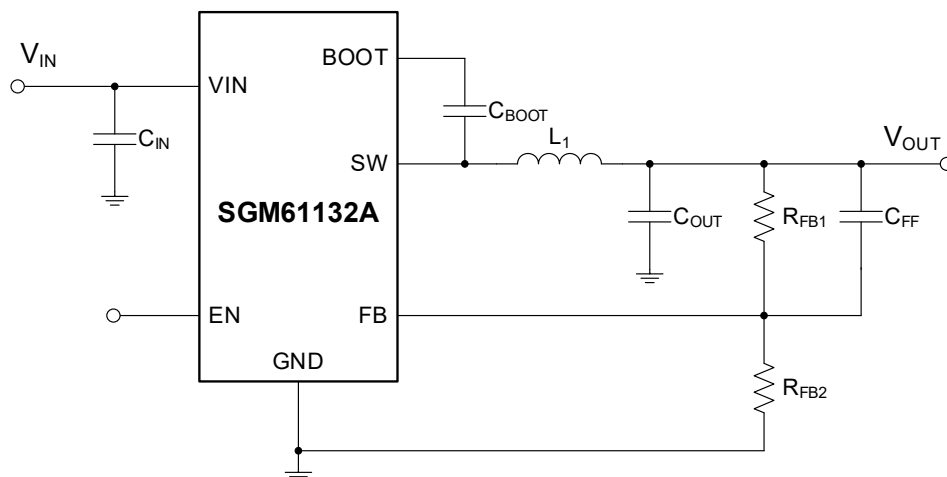
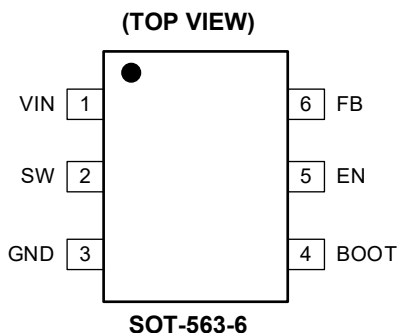


Figure 1. Typical Application Circuit

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	VIN	P	Supply Input. Connect VIN to a power source with 4.5V to 17V voltage range. Decouple VIN to GND as close as possible with a high frequency, low ESR ceramic capacitor (X5R or higher grade is recommended).
2	SW	P	Switching Node. Connection point of the internal converter lower and upper power MOSFETs. Connect this pin to the output inductor and the bootstrap capacitor.
3	GND	G	Device Ground Reference Pin.
4	BOOT	P	Bootstrap Pin. Bootstrap supply for high-side driver. Connect a 0.1µF ceramic capacitor between BOOT and SW pins.
5	EN	I	Active-High Enable Input. Pull up to a logic-high voltage (not higher than 17V) to enable the device, pull down to disable it. Input UVLO level can be programmed using a resistor divider from VIN.
6	FB	I	Feedback Pin for Setting the Output Voltage. Tap an output feedback resistor divider to this pin.

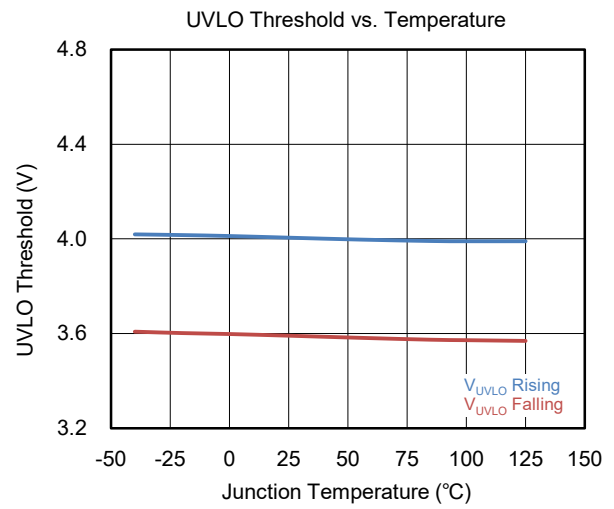
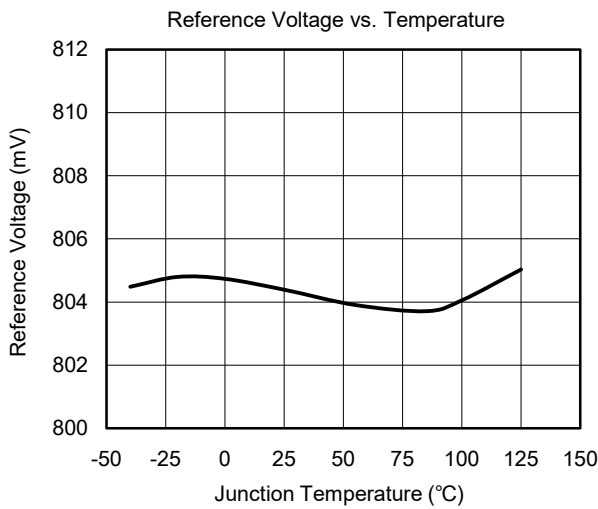
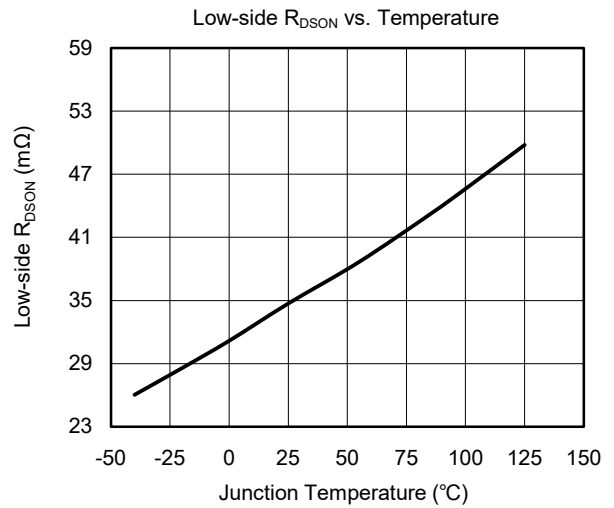
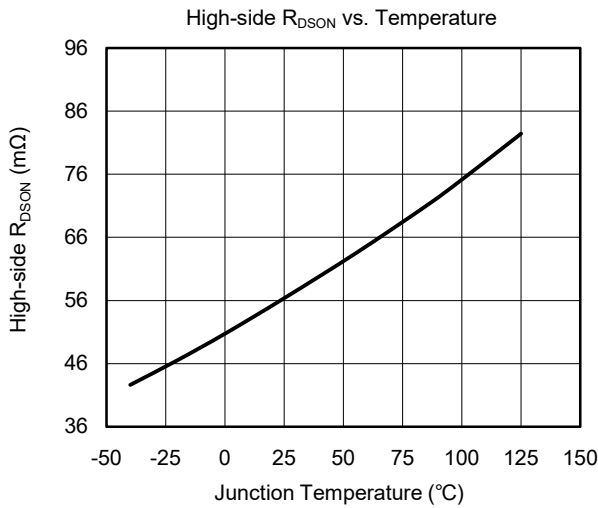
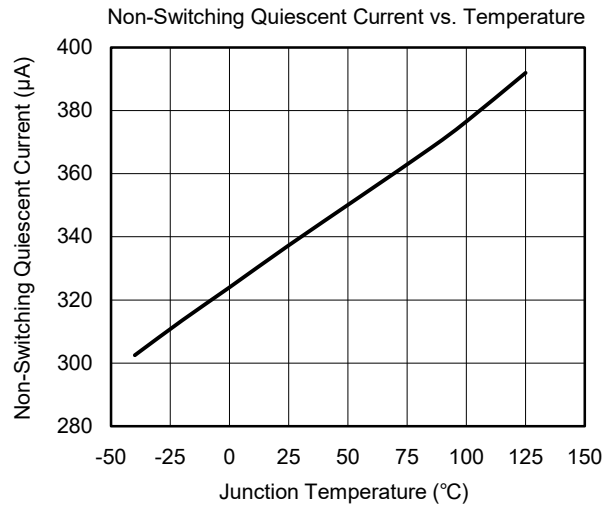
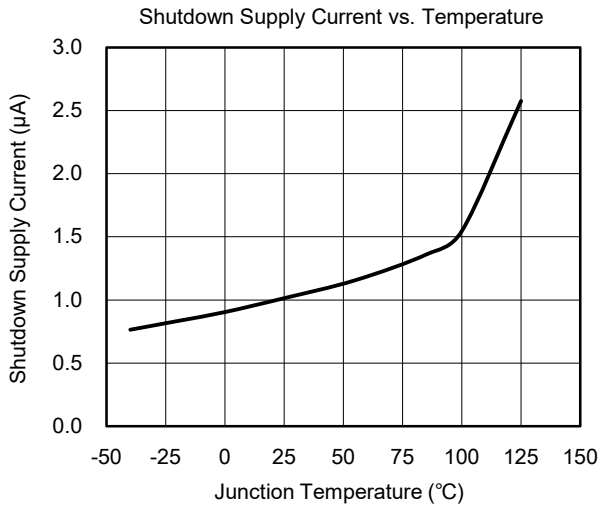
NOTE: I = Input, P = Power, G = Ground.

ELECTRICAL CHARACTERISTICS(V_{IN} = 12V, T_J = -40°C to +125°C, typical values are measured at T_J = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current						
Operating - Non-Switching Supply Current	I _{IN}	V _{IN} current, V _{EN} = 5V, V _{FB} = 1V		340	550	μA
Shutdown Supply Current	I _{SD}	V _{IN} current, V _{EN} = 0V		1	3.6	μA
Logic Threshold						
EN High-Level Input Voltage	V _{ENH}	EN Rising		1.2	1.3	V
EN Low-Level Input Voltage	V _{ENL}	EN Falling	0.9	1.05		V
EN Pin Resistance to GND	R _{EN}	V _{EN} = 5V		1.2		MΩ
Reference Voltage						
Reference Voltage	V _{REF}	T _J = +25°C	788	806	826	mV
		T _J = -40°C to +125°C	786	806	828	
FB Input Current	I _{FB}	V _{FB} = 1V		0.01	0.1	μA
MOSFET						
High-side Switch On-Resistance	R _{DSON_HS}			56		mΩ
Low-side Switch On-Resistance	R _{DSON_LS}			35		mΩ
Current Limit						
Low-side Current Limit	I _{OCL}	V _{OUT} = 3.3V, L ₁ = 3.3μH, T _J = +25°C	2.6	4.2	5.9	A
Thermal Shutdown						
Thermal Shutdown Threshold	T _{SD}			160		°C
Thermal Shutdown Hysteresis	T _{SD_HYS}			30		°C
On-Time Timer Control						
Minimum Off-Time	t _{OFF_MIN}	V _{FB} = 0.6V		300		ns
Soft-Start						
Soft-Start Time	t _{SS}	Internal soft-start time		1.0		ms
Frequency						
Switching Frequency	f _{SW}			500		kHz
Output Under-Voltage						
Output UVP Threshold	V _{UVP}	Hiccup detect threshold, percentage of V _{REF}		60%		
Hiccup Delay	t _{HICCUP_WAIT}			24		μs
Hiccup Time before Restart	t _{HICCUP_RE}			15		ms
UVLO						
UVLO Threshold	V _{UVLO}	V _{IN} rising		4.0	4.4	V
		V _{IN} falling	3.2	3.6		
UVLO Threshold Hysteresis	V _{UVLO_HYS}	Hysteresis		0.4		V

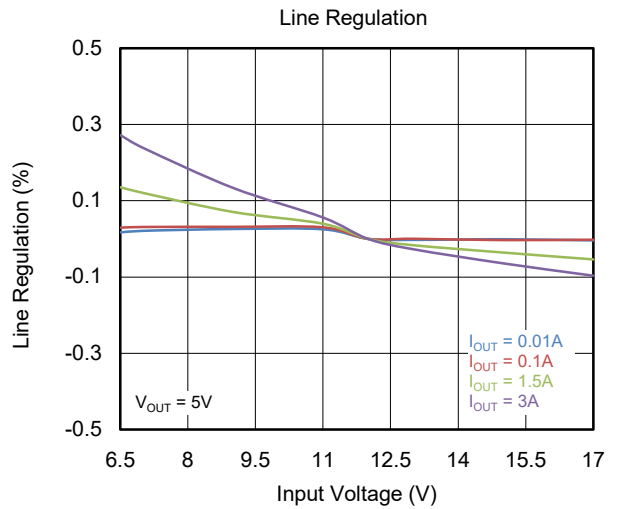
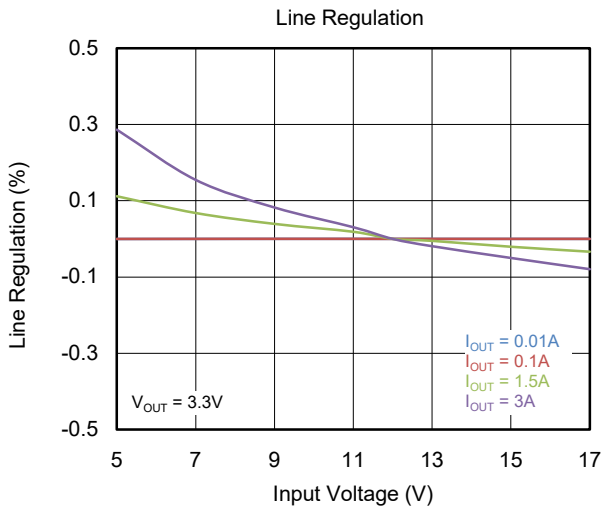
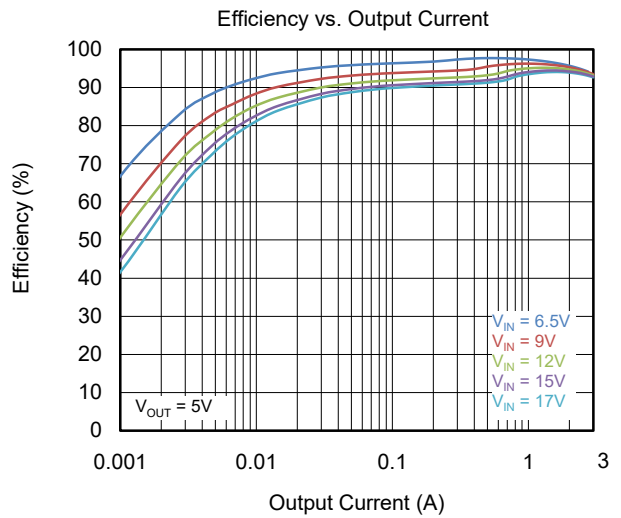
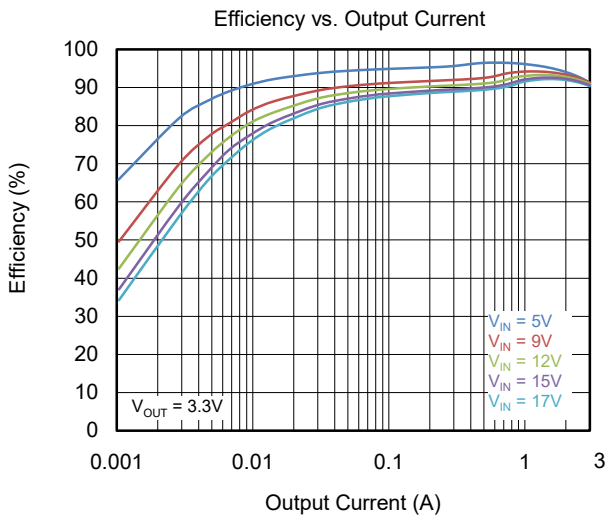
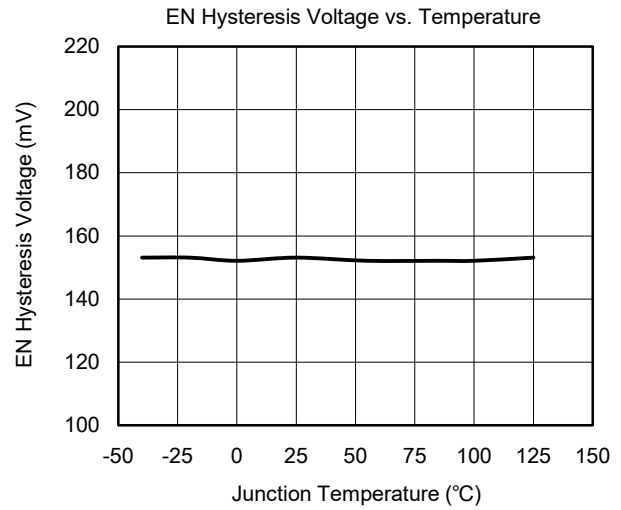
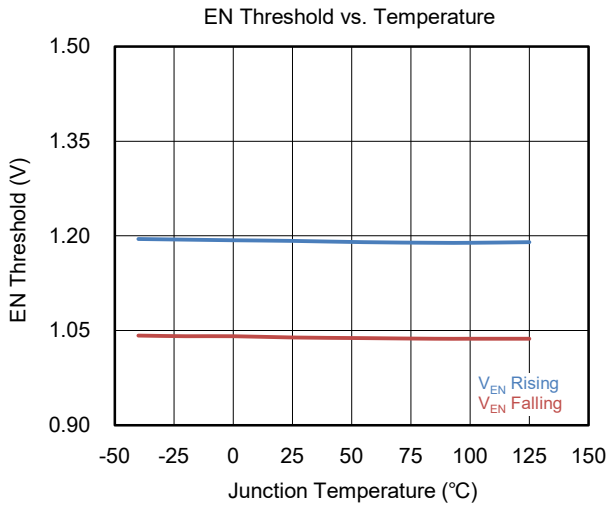
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = +25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{OUT} = 3.3\text{V}$, $L_1 = 3.3\mu\text{H}$ and $C_{OUT} = 22\mu\text{F} \times 2$, unless otherwise noted.



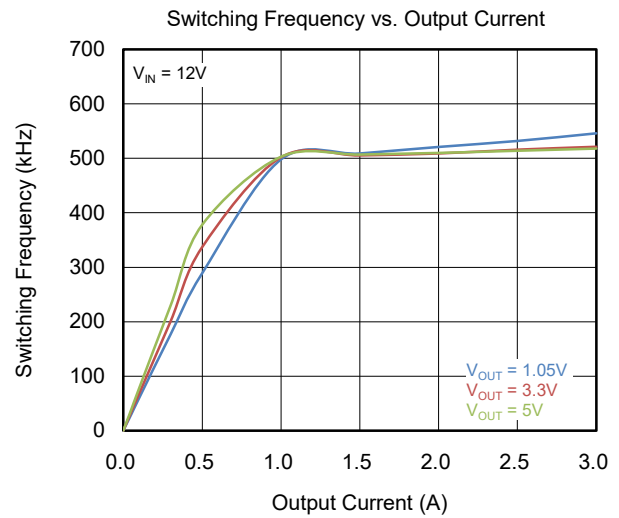
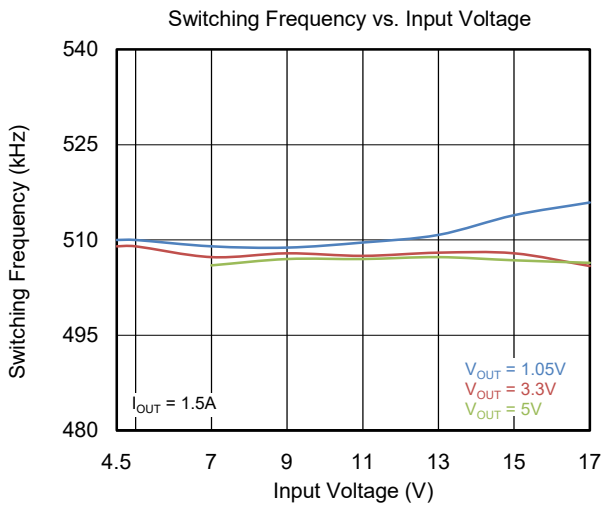
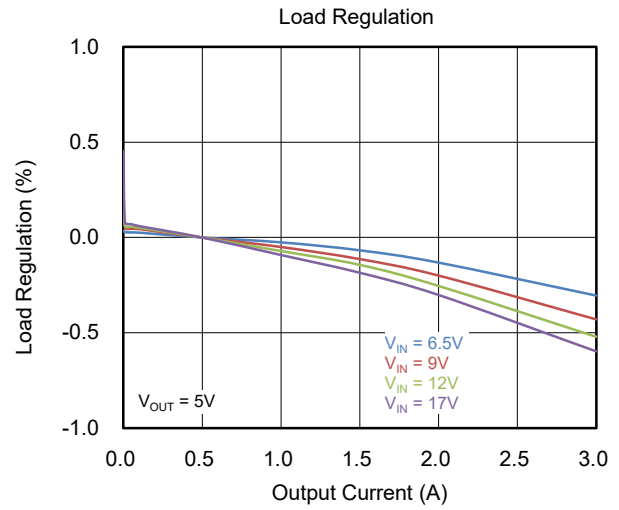
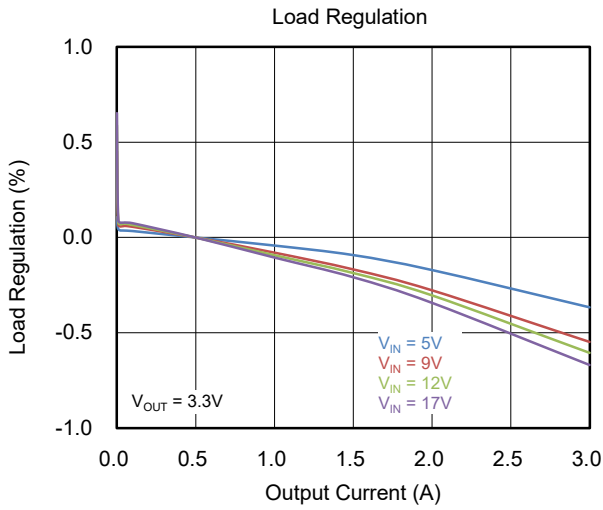
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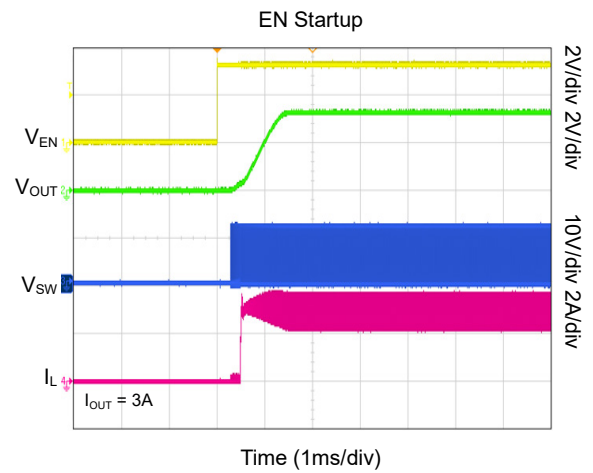
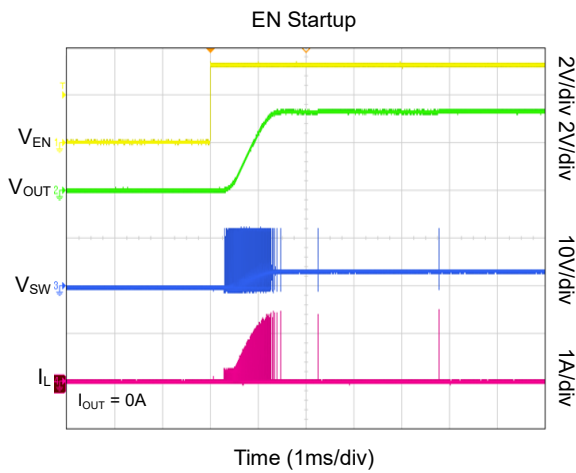
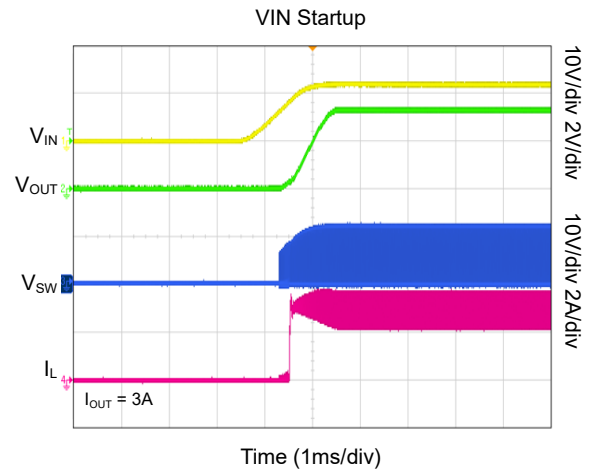
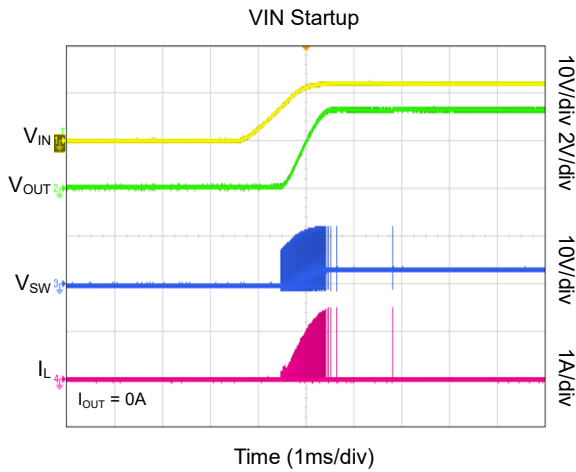
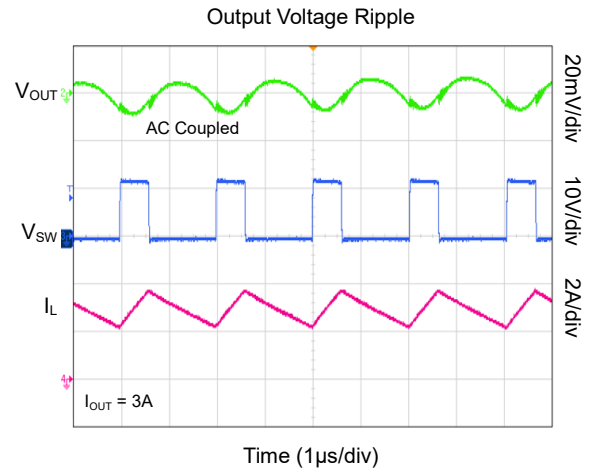
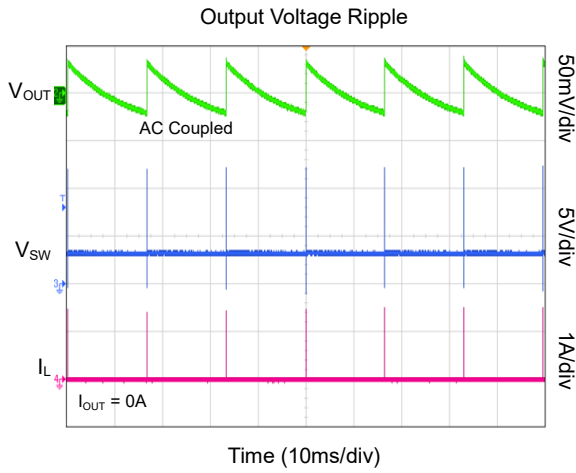
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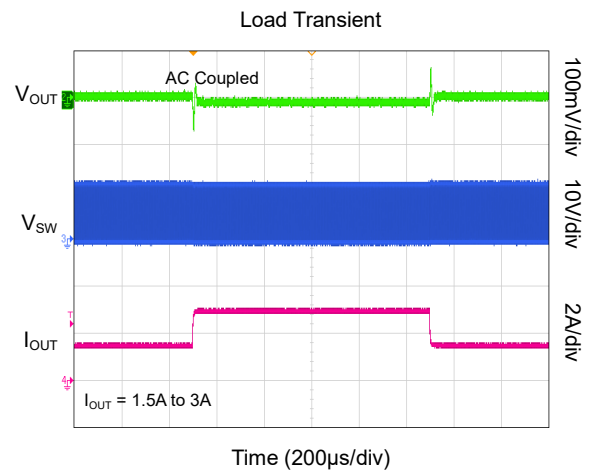
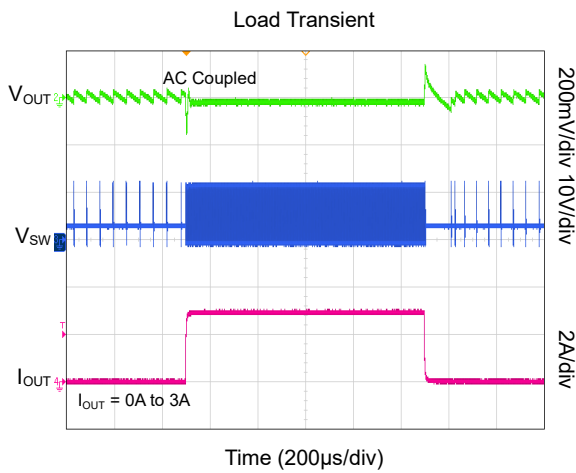
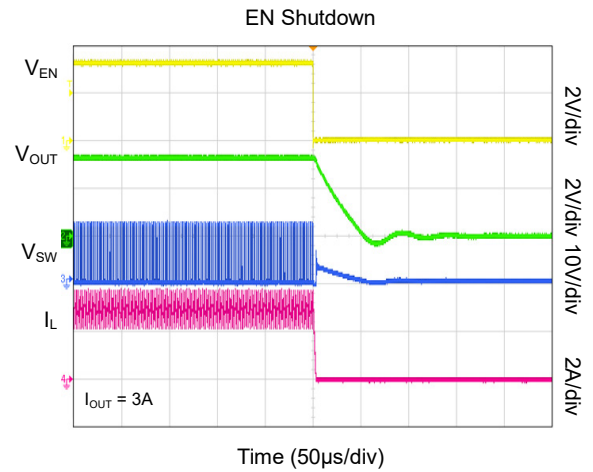
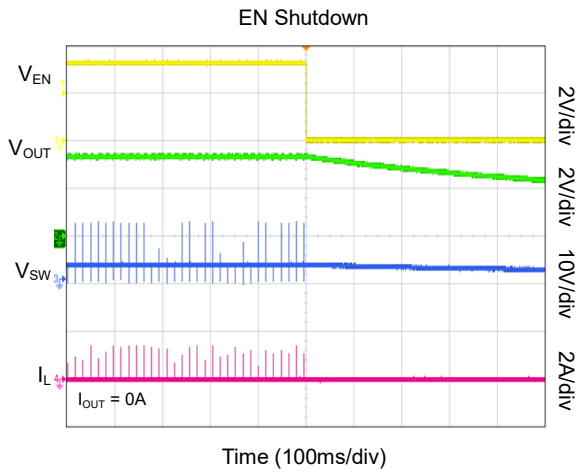
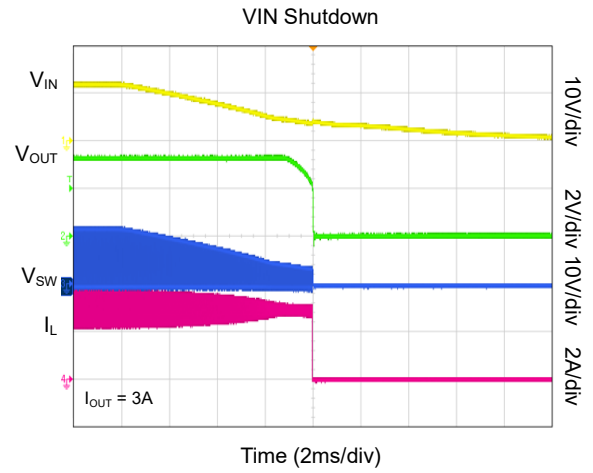
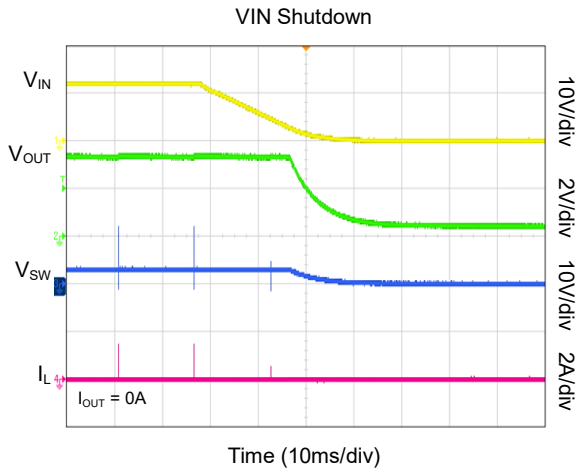
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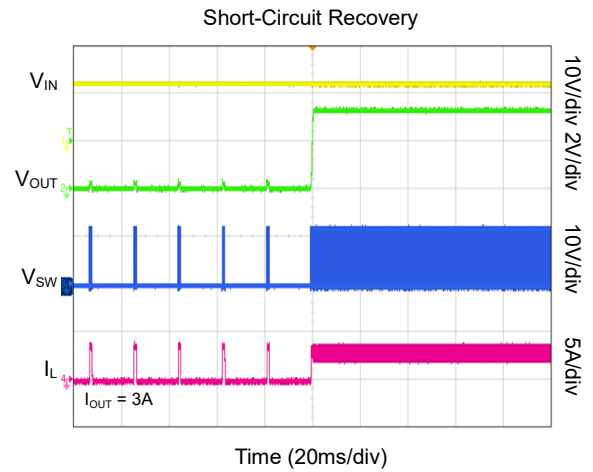
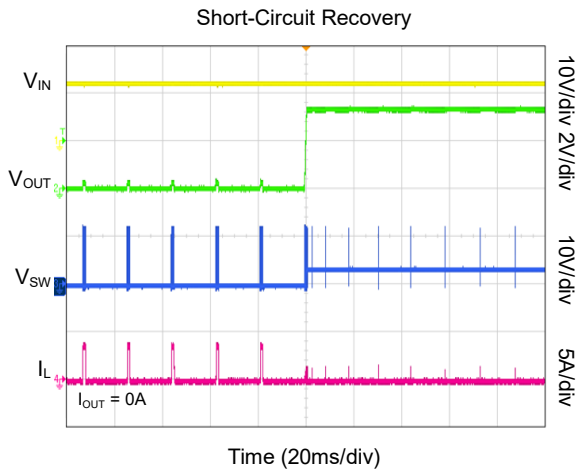
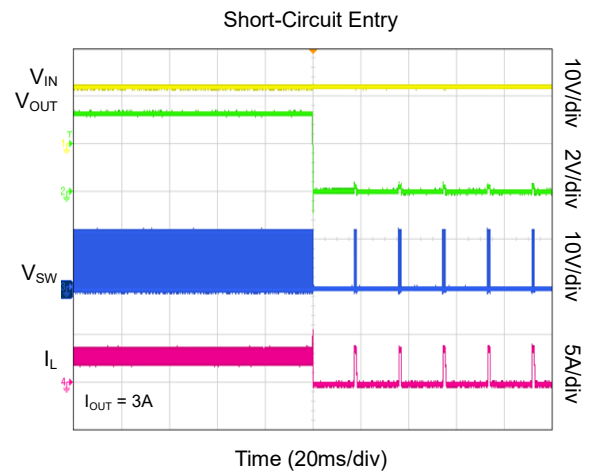
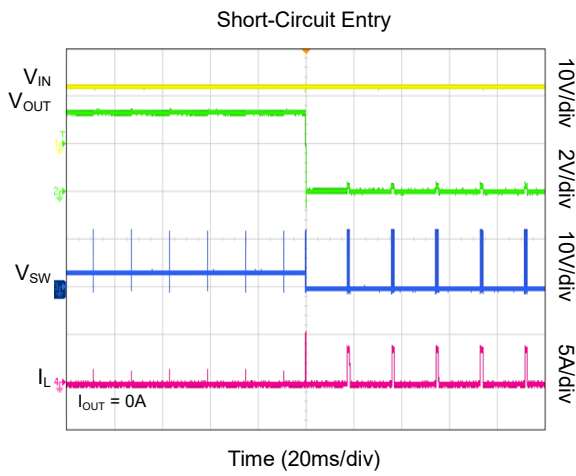
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FUNCTIONAL BLOCK DIAGRAM

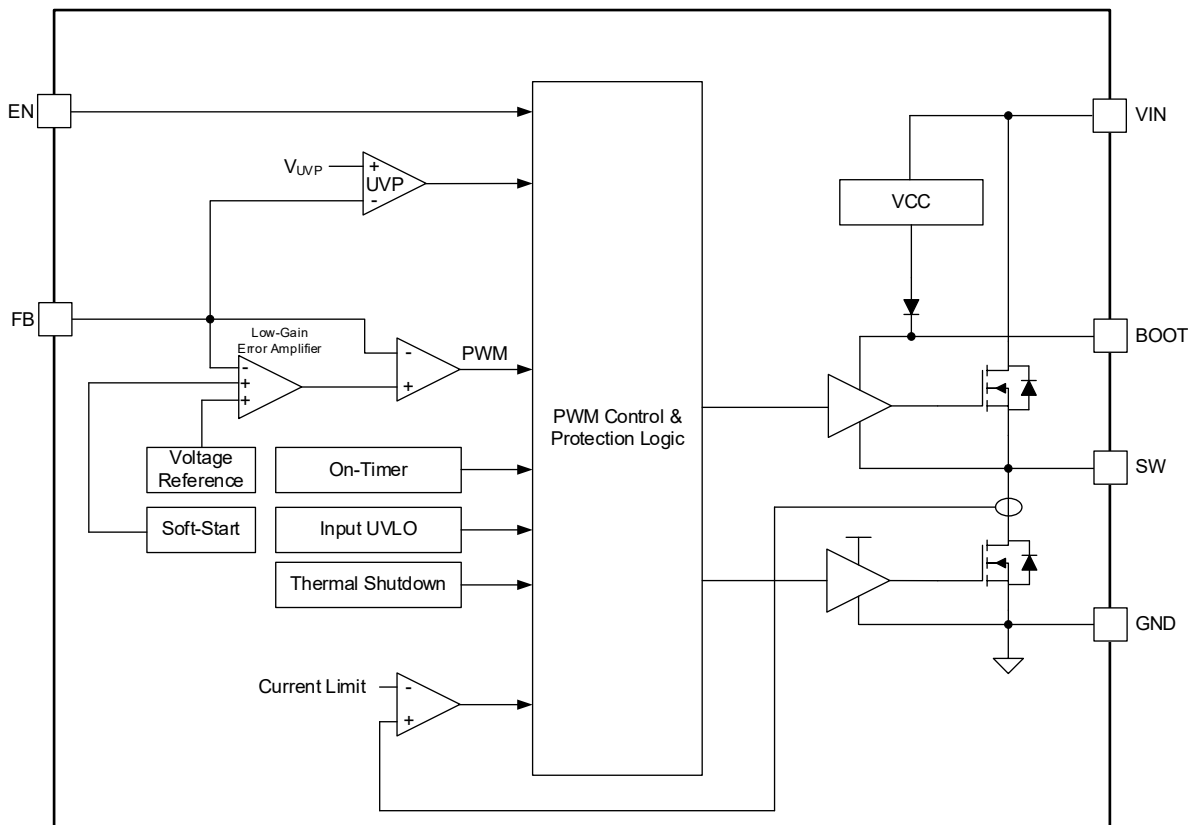


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61132A is a 17V/3A synchronous Buck converter with over-current, short-circuit protections and thermal shutdown with auto recovery.

Adaptive Constant On-Time Control

In conventional voltage mode control (VMC) or current mode control (CMC) converters, a fixed frequency clock timing signal generates a saw-tooth ramp that is compared with the compensation network output to adjust the PWM duty cycle (on-time) as control variable and regulate the output voltage and/or current feedback(s) to govern the control variable and keep the output regulated with fast reaction to load or V_{IN} variations. The existence of the compensator in VMC or CMC converter inherently introduces some delay in the loop response.

Unlike VMC or CMC, the adaptive constant on-time (ACOT) control is a hysteretic mode control without clock signal. Each switching cycle is started with a relative constant on-time pulse when an internal comparator senses that the output voltage drops below the desired output voltage. Output voltage is sensed by the feedback (FB) pin through an output resistor divider and is compared to the internal reference voltage (V_{REF}) with a low gain error amplifier. The amplifier output is sent to a comparator and when the feedback voltage (V_{FB}) falls below amplifier output, the comparator triggers the on-time control logic that turns on the high-side switch. ACOT control is able to dynamically adjust the on-time duration based on the input voltage and output voltage so that it can achieve relative constant frequency during steady state operation, which minimizes the EMI interference at some sensitive bands of certain frequencies in the system. An internal ramp is added to reference voltage to simulate output ripple, so it supports low ESR output capacitors applications.

Enable

The voltage on the EN pin provides the precision enable and disable of SGM61132A. The device will enable if the EN pin voltage exceeds the enable threshold of 1.2V and V_{IN} exceeds its UVLO threshold. The device will disable if the EN voltage is externally pulled low or the V_{IN} pin voltage falls below its UVLO threshold. The EN pin cannot be left floating and can be connected to V_{IN} to enable the device if V_{IN} is not higher than 17V.

An external input UVLO adjustment circuit is recommended in Figure 3. The EN input can be driven by an external logic signal to facilitate system sequencing and protection. If $V_{EN} < 1.05V$ (TYP), the device will shut down. Only if $V_{EN} > 1.2V$ (TYP), the device will start operation.

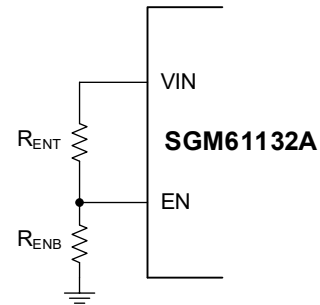


Figure 3. System UVLO by Enable Divider

Bootstrap Voltage (BOOT)

To power the upper switch gate driver, a voltage higher than V_{IN} is needed. Bootstrap technique is used to provide this voltage from the switching node by using a 0.1μF bootstrap capacitor between SW and BOOT pins along with an internal bootstrap diode. The voltage is internally regulated for driving the high-side switch. An X5R or X7R ceramic capacitor is recommended for C_{BOOT} to have stable capacitance against temperature and voltage variations.

Output Voltage Programming

The output voltage is set by a resistor divider between V_{OUT} and GND that is tapped to the FB pin. It is recommended to use 1% or higher quality resistors with low thermal tolerance for an accurate and thermally stable output voltage.

Use Equation 1 and Figure 1 to calculate the output voltage. Lower divider resistor values increase loss and reduce light-load efficiency. Consider larger resistors to improve efficiency at light-load, and start with 10kΩ for the bottom resistor (R_{FB2}). Note that if R_{FB1} is too high (> 1MΩ), the FB pin leakage current and other noises can easily affect the accuracy and performance of the regulator.

$$V_{OUT} = V_{FB} \times \left[\frac{R_{FB1}}{R_{FB2}} + 1 \right] \tag{1}$$

DETAILED DESCRIPTION (continued)

Internal Voltage Reference and Soft-Start

The SGM61132A device has an internal 0.806V reference (V_{REF}) to program the output at the desired level. When the converter starts (or is enabled), an internal ramp voltage begins to rise from near 0V to slightly above 0.806V with a ramp time of 1ms. The lower of V_{REF} and this ramp is used as reference for the error amplifier. Therefore, the ramp provides a soft-start for the output during startup. The soft-start is needed to avoid high inrush currents caused by rapid increase of output voltage across output capacitors and the load.

Operation with Pulse-Skip Mode

When SGM61132A operates in discontinuous conduction mode (DCM) with light load, it goes into the pulse-skip mode in which internal power dissipation is significantly reduced. Moreover, the operating frequency starts to drop depending on the load.

The details are explained in Figure 4 that shows the timings of the COT control in DCM. Inductor current (I_L) is monitored with a zero-crossing detector and when I_L crosses the zero, both high-side and low-side MOSFETs are turned off (if $V_{FB} > V_{REF_EA}$). They will not turn on again until the V_{FB} falls below V_{REF_EA} and triggers a new on-time pulse. During this off-time period, all non-essential circuits are shut down to minimize losses and the load is supplied by the output capacitor stored energy. The control circuitry wakes up when the new on-pulse is triggered.

Over-Current and Short-Circuit Protection

The SGM61132A supports overload mode. When the output current continues overload during the system power-up, the SGM61132A exports the maximized power and limits the maximum valley current of the low-side FET switch. The device keeps in cycle-by-cycle limit to obtain the system's power request. The SGM61132A does not shut down until the device heats and then goes to thermal shutdown. As the load increases continuously, the output voltage decreases. If SS is ready and the FB voltage drops to 60% of V_{REF} , hiccup current-protection mode is activated. In hiccup mode, the regulator is shut down and kept off for 15ms typically before the SGM61132A tries to start again. If over-current or a short-circuit fault condition still exists, the hiccup mode will repeat until the fault condition is removed. Hiccup mode can help to reduce power dissipation and prevent overheating and potential damage to the device.

Thermal Shutdown

If the junction temperature exceeds +160°C (TYP), the device is forced to stop switching. It will recover automatically when T_J falls below the recovery threshold.

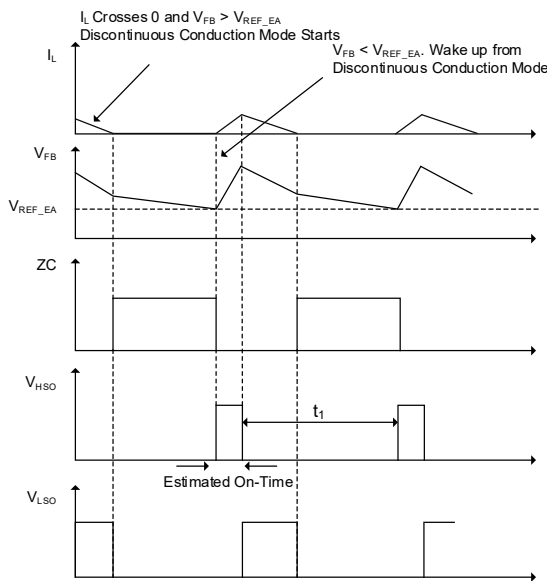


Figure 4. Pulse-Skip Mode (DCM)

APPLICATION INFORMATION

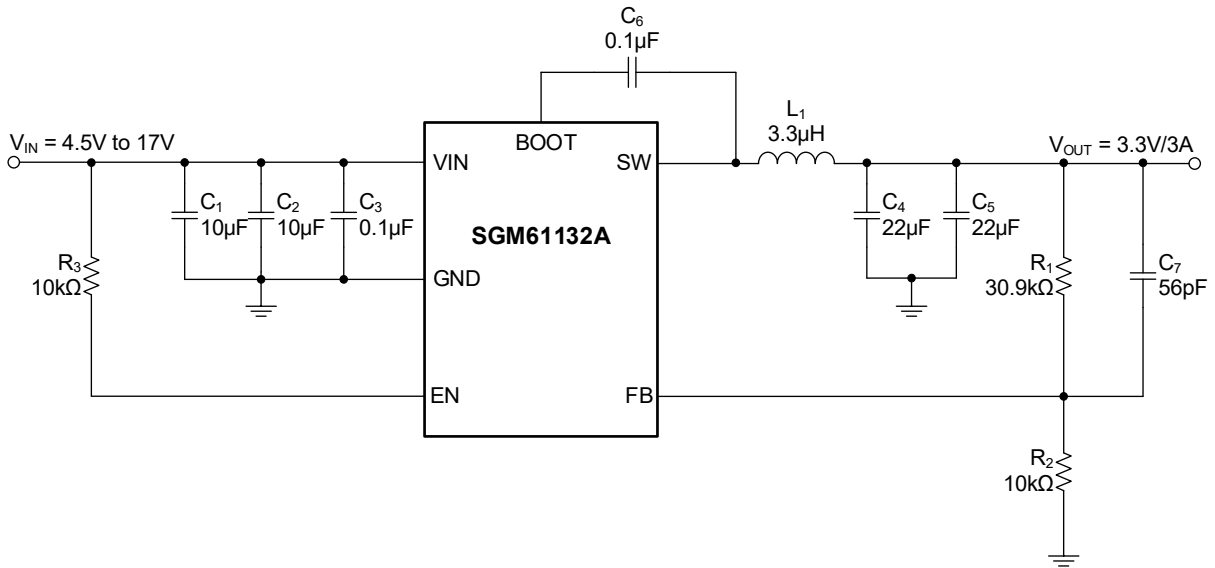


Figure 5. A Reference Design for 3.3V/3A Application

The design method and component selection for the SGM61132A Buck converter is explained in this section. Schematic of a basic design is shown in Figure 5. Only a few external components are needed to provide a constant output voltage from a wide input voltage range.

The external components are designed based on the application requirements and device stability. Some suitable output filters (L and C_{OUT}) along with C_{FF} and divider resistor values are provided in Table 1 to simplify component selection.

Table 1. Recommended Component Values

V _{OUT} (V)	L ₁ (μH)	C ₄ + C ₅ (μF)	R ₁ (kΩ)	R ₂ (kΩ)	C ₇ (pF)
0.85	1.2	44	0.55	10	56
1.05	1.2	44	3	10	56
3.3	3.3	44	30.9	10	56
5	4.7	44	52.3	10	56

Design Requirements

A typical application circuit for the SGM61132A as a Buck converter is shown in Figure 5. It is used for converting a 4.5V to 17V supply voltage to a lower voltage level supply voltage (3.3V) suitable for the system. The design parameters given in Table 2 are used for this design example.

Table 2. Design Parameters

Design Parameters	Example Values
Input Voltage	12V (TYP), 4.5V to 17V
Input Ripple Voltage	240mV, 2% of V _{IN_TYP}
Output Voltage	3.3V
Output Voltage Ripple	66mV, 2% of V _{OUT}
Output Current Rating	3A
Transient Response, 1.5A to 3A Load Step	165mV, 5% of V _{OUT}
Operation Frequency	500kHz

Input Capacitor Selection

A high-quality ceramic capacitor (X5R or X7R or better dielectric grade) must be used for input decoupling of the SGM61132A. At least 3μF of effective capacitance (after de-ratings) is needed on the VIN input. In some applications, additional bulk capacitance may also be required for the VIN input, for example, when the SGM61132A is more than 5cm away from the input source. The VIN capacitor ripple current rating must also be greater than the maximum input current ripple. The input current ripple can be calculated using Equation 2 and the maximum value occurs at 50% duty cycle. Using the design example values, I_{OUT} = 3A, yields an RMS input ripple current of 1.339A.

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT})}{V_{IN}}} = I_{OUT} \times \sqrt{D \times (1 - D)} \quad (2)$$

APPLICATION INFORMATION (continued)

For this design, a ceramic capacitor with at least 25V voltage rating is required to support the maximum input voltage. So, two 10 μ F/25V capacitors are selected for VIN to cover all DC bias, thermal and aging de-ratings. The input capacitance determines the regulator input voltage ripple. This ripple can be calculated from Equation 3. In this example, the total effective capacitance of the 2 \times 10 μ F/25V capacitor is around 8 μ F at 12V input, and the input voltage ripple is 149.6mV.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (3)$$

It is recommended placing an additional small size 0.1 μ F ceramic capacitor right beside VIN and GND pins for high frequency filtering.

Inductor Selection

Equation 4 is conventionally used to calculate the output inductance of a Buck converter. The ratio of inductor current ripple (ΔI_L) to the maximum output current (I_{OUT}) is represented as K_{IND} factor ($\Delta I_L/I_{OUT}$). The inductor ripple current is bypassed and filtered by the output capacitor and the inductor DC current is passed to the output. Inductor ripple is selected based on a few considerations. The peak inductor current ($I_{OUT} + \Delta I_L/2$) must have a safe margin from the saturation current of the inductor in the worst-case conditions especially if a hard-saturation core type inductor (such as ferrite) is chosen. The ripple current also affects the selection of the output capacitor. C_{OUT} RMS current rating must be higher than the inductor RMS ripple. Typically, a 40% ripple is selected ($K_{IND} = 0.4$).

$$L = \frac{V_{IN_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN_MAX} \times f_{SW}} \quad (4)$$

In this example, the calculated inductance will be 4.43 μ H with $K_{IND} = 0.4$, for compact application scenario a 3.3 μ H is selected. The ripple, RMS and peak inductor current calculations are summarized in Equations 5, 6 and 7 respectively.

$$\Delta I_L = \frac{V_{IN_MAX} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN_MAX} \times f_{SW}} \quad (5)$$

$$I_{L_RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}} \quad (6)$$

$$I_{L_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (7)$$

Note that during startup, load transients or fault conditions, the peak inductor current may exceed the calculated I_{L_PEAK} . Therefore, it is always safer to choose the inductor saturation current higher than the switch current limit.

Output Capacitor Selection

The output capacitors and inductor filter the AC part of the PWM switching voltage and provide an acceptable level of output voltage ripple superimposed on the desired output DC voltage. Additionally, the capacitors store energy to assist in maintaining output voltage regulation during load transient. The output voltage ripple (ΔV_{OUT}) depends on the output capacitor value at the operating voltage, temperature ($^{\circ}$ C) and its parasitic parameters (ESR and ESL):

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{V_{IN} - V_{OUT}}{L} \times ESL + \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}} \quad (8)$$

The voltage rating of the output capacitors should be selected with enough margins to ensure that capacitance drop (voltage and temperature de-rating) is not significant.

The type of output capacitors will determine which terms of Equation 8 are dominant. For ceramic output capacitors, the ESR and ESL are virtually zero, so the output voltage ripple will be dominated by the capacitive term. For electrolytic output capacitors, the value of capacitance is relatively high, and compared with ESR and ESL terms, the third term in Equation 8 can be ignored.

To reduce the voltage ripple, either inductance or the total capacitance is increased. Higher quality capacitors, larger inductance or using parallel capacitors can help reduce the output ripple in a design using electrolytic output capacitors.

APPLICATION INFORMATION (continued)

The ESR of some commercial electrolytic capacitors can be quite high, and it is recommended using quality capacitors with the ESR or the total impedance clearly documented in the datasheet. ESR of an electrolytic capacitor may increase significantly at cold ambient temperatures with a factor of 10 or so, which increases the ripple and can deteriorate the regulator stability.

The transient response of the regulator also depends on the quantity and type of output capacitors. In general, reducing the ESR of the output capacitance will lead to a better transient response. The ESR can be minimized by simply adding more capacitors in parallel or by using higher quality capacitors. When a fast load transient of magnitude ΔI_L and rate of di/dt occurs, the output voltage will jump or dip by a transient magnitude of ΔV_{OUT} :

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{di}{dt} \times ESL \quad (9)$$

Right after the transient, the inductor current remains almost constant especially for larger inductors and the transient current is carried by the capacitor. The output voltage will deviate from its nominal value for a short time depending on the system bandwidth, the inductor and the output capacitance. In this example, according to Table 1, $2 \times 22\mu\text{F}/16\text{V}$ X5R ceramic capacitors with $2\text{m}\Omega$ of ESR can meet the above conditions.

Bootstrap Capacitor Selection

Use a $0.1\mu\text{F}$ high-quality ceramic capacitor (X5R or X7R) with 10V or higher voltage rating for the bootstrap capacitor (C_6).

Output Voltage Setting

Use an external resistor divider (R_1 and R_2) to set the output voltage using Equation 10:

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (10)$$

where $V_{REF} = 0.806\text{V}$ is the internal reference. For example, by choosing $R_2 = 10\text{k}\Omega$, the R_1 value for 3.3V output will be calculated as $30.94\text{k}\Omega$.

Feed-Forward Capacitor Selection

The SGM61132A contains an internal compensation circuit, an internal ramp is added to reference voltage to simulate output ripple. For ultra-low output capacitance ESR (ceramic capacitor) applications, it is recommended adding a 56pF feed-forward capacitor (C_7) to provide a low-impedance path for output voltage ripple and ensure minimal phase shift of the voltage ripple at the feedback node while maintaining acceptable transient response.

APPLICATION INFORMATION (continued)

Layout Guide

PCB is an essential element of any switching power supply. The converter operation can be significantly disturbed due to the existence of the large and fast rising/falling voltages that can couple through stray capacitances to other signal paths, and also due to the large and fast changing currents that can interact through parasitic magnetic couplings, unless those interferences are minimized and properly managed in the layout design. Insufficient conductance in copper traces for the high current paths results in high resistive losses in the power paths and voltage errors. The following guidelines provided here are necessary to design a good layout:

- ◆ Bypass VIN pin to GND pin with low-ESR ceramic capacitors (X5R or X7R better dielectric) placed as close as possible to VIN pin.
- ◆ Use short, wide and direct traces for high-current connections (VIN, SW and GND).
- ◆ Keep the BOOT-SW voltage path as short as possible.
- ◆ Place the feedback resistors as close as possible to the FB pin that is sensitive to noise.
- ◆ Minimize the area and path length of the loop formed by VIN pin, bypass capacitors connections and SW pin.

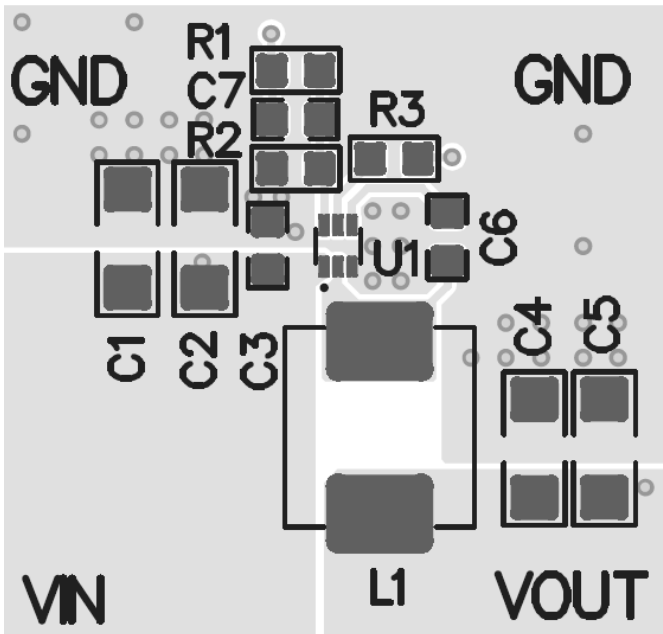


Figure 6. PCB Top Layer

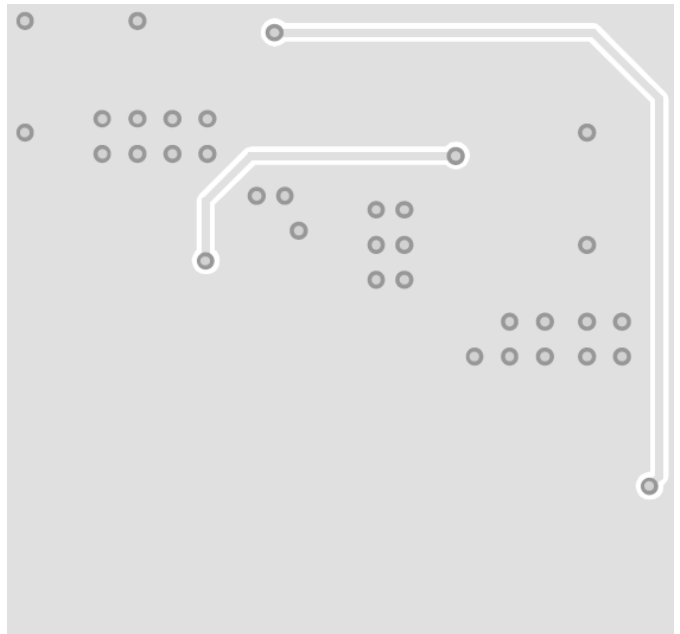


Figure 7. PCB Bottom Layer

REVISION HISTORY

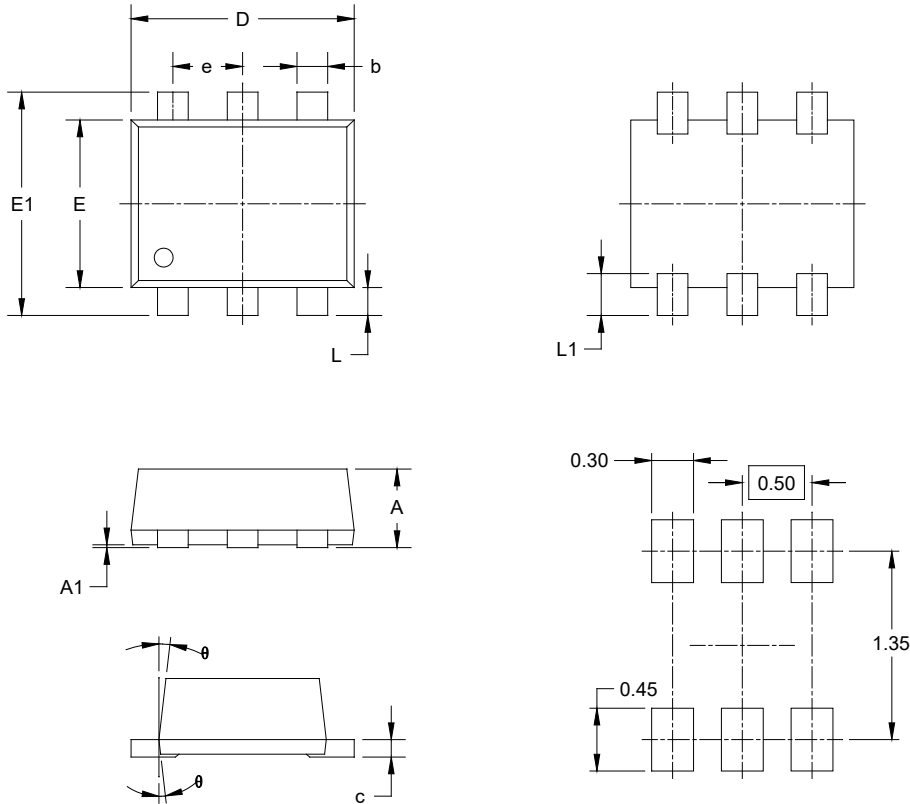
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

AUGUST 2024 – REV.A to REV.A.1	Page
Updated the Features section.....	1
Updated the Typical Performance Characteristics section	7, 9
Updated the Enable and Output Capacitor Selection sections	12, 15

Changes from Original (JULY 2024) to REV.A	Page
Changed from product preview to production data.....	All

PACKAGE OUTLINE DIMENSIONS

SOT-563-6



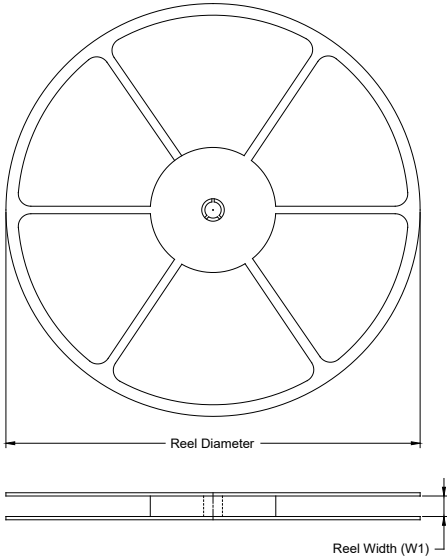
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.525	0.600	0.021	0.024
A1	0.000	0.050	0.000	0.002
b	0.170	0.270	0.007	0.011
c	0.090	0.180	0.004	0.007
D	1.500	1.700	0.059	0.067
E	1.100	1.300	0.043	0.051
E1	1.500	1.700	0.059	0.067
e	0.450	0.550	0.018	0.022
L	0.100	0.300	0.004	0.012
L1	0.200	0.400	0.008	0.016
θ	9° REF		9° REF	

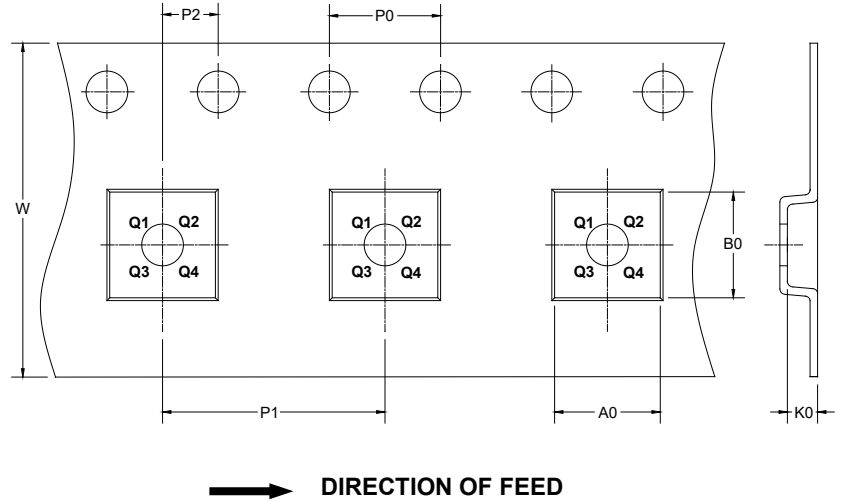
NOTES:
 1. Body dimensions do not include mode flash or protrusion.
 2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

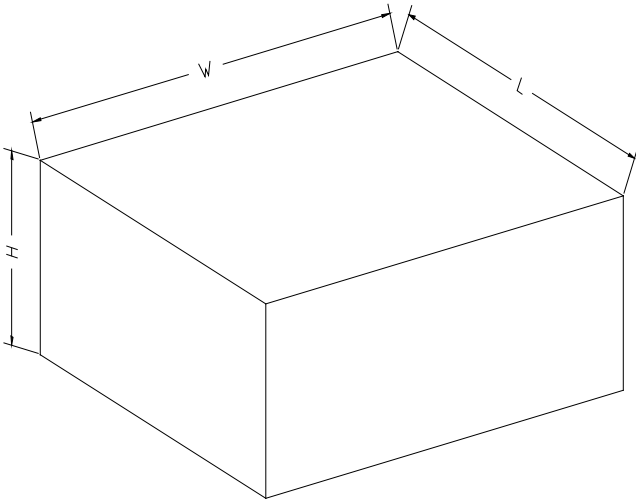
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-563-6	7"	9.5	1.78	1.78	0.69	4.0	4.0	2.0	8.0	Q3

DD0001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18

DD0002