SGM48211
120V Boot, 4A Peak, High Frequency High-side and Low-side Driver

GENERAL DESCRIPTION

The SGM48211 is a half-bridge MOSFET driver with 4A peak source and sink output current capability, which makes it possible to drive large power MOSFETs with minimized switching losses. The two channels of high-side and low-side are totally independent with 3ns (TYP) delay matching between the turn-on and turn-off of each other.

The maximum withstanding voltage of the input stage of SGM48211 is 20V. Due to the -10V_{DC} voltage endurance capacity of its input stage, the driver has enhanced robustness and can be interfaced to pulse transformers directly without using rectifier diodes. With a wide input hysteresis, the device can receive analog or digital PWM signals with improved noise immunity.

A 120V rated bootstrap diode is integrated internally to save the external diode and reduce PCB dimension size.

Under-voltage lockout (UVLO) is integrated in both the high-side and the low-side drivers. The output of each channel is forced low if the corresponding driving voltage falls below the specified threshold.

The SGM48211 is available in Green SOIC-8, SOIC-8 (Exposed Pad) and TDFN-4×4-8AL packages.

FEATURES

- **Wide Operating Range: 8V to 17V**
- **Drive Two N-MOSFETs Configured in Half Bridge**
- **Maximum Blocking Voltage: 120V DC**
- **Integrated Internal Bootstrap Diode for Cost Saving**
- **4A Peak Sink and Source Currents**
- **-10V to 20V Tolerance of Input Pins**
- **COMS/TTL Compatible Inputs**
- **6.5ns (TYP) Rise Time and 4.5ns (TYP) Fall Time with 1000pF Load**
- **Propagation Delay Time: 31ns (TYP)**
- **Delay Matching: 3ns (TYP)**
- **UVLO Functions for Both High-side and Low-side Drivers**
- **-40℃ to +140℃ Operating Junction Temperature Range**
- **Available in Green SOIC-8, SOIC-8 (Exposed Pad) and TDFN-4×4-8AL Packages**

APPLICATIONS

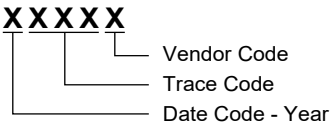
Power Converters in 48V or Lower Systems Used in Telecom, Datacom, Portable Storage, etc.
Half-Bridge, Full-Bridge, Push-Pull, Synchronous-Buck and Forward Converters
Synchronous Rectifiers
Class-D Audio Amplifiers

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM48211	SOIC-8	-40℃ to +140℃	SGM48211XS8G/TR	SGM 48211XS8 XXXXX	Tape and Reel, 4000
	SOIC-8 (Exposed Pad)	-40℃ to +140℃	SGM48211XPS8G/TR	SGM 48211XPS8 XXXXX	Tape and Reel, 4000
	TDFN-4×4-8AL	-40℃ to +140℃	SGM48211XTGW8G/TR	SGM48211 XTGW8 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{DD} (1), V_{HB} - V_{HS} ..... -0.3V to 20V
Input Voltages on LI and HI, V_{LI}, V_{HI} ..... -10V to 20V
LO Output Voltage, V_{LO} .....-0.3V to V_{DD} + 0.3V
HO Output Voltage, V_{HO}.....V_{HS} - 0.3V to V_{HB} + 0.3V
HS Voltage, V_{HS}
DC ..... -1V to 115V
Repetitive Pulse < 100ns .....-(24V - V_{DD}) to 115V
HB Voltage, V_{HB} ..... -0.3V to 120V
Package Thermal Resistance
SOIC-8, θ_{JA} ..... 104.9℃/W
SOIC-8, θ_{JB} ..... 50.7℃/W
SOIC-8, θ_{JC} ..... 49.4℃/W
SOIC-8 (Exposed Pad), θ_{JA}..... 37.9℃/W
SOIC-8 (Exposed Pad), θ_{JB}..... 14.2℃/W
SOIC-8 (Exposed Pad), $\theta_{JC\ (TOP)}$ ..... 59.3℃/W
SOIC-8 (Exposed Pad), $\theta_{JC\ (BOT)}$ ..... 4.3℃/W
TDFN-4×4-8AL, θ_{JA}..... 32.6℃/W
TDFN-4×4-8AL, θ_{JB}..... 11.5℃/W
TDFN-4×4-8AL, $\theta_{JC\ (TOP)}$..... 33.9℃/W
TDFN-4×4-8AL, $\theta_{JC\ (BOT)}$ ..... 2.8℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....2000V
CDM 1000V

NOTE:
1. All voltages are with reference to VSS. Positive and negative currents are defined by flowing into and out of the specified terminal respectively.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{DD}, V_{HB} - V_{HS} .....8V to 17V
HS Voltage, V_{HS} .....-1V to 105V
HB Voltage, V_{HB} .....V_{HS} + 8V to V_{HS} + 17V
HB Voltage, V_{HB} .....V_{DD} - 1V to 110V
HS Voltage Slew Rate.....50V/ns (MAX)
Operating Junction Temperature Range ..... -40℃ to +140℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

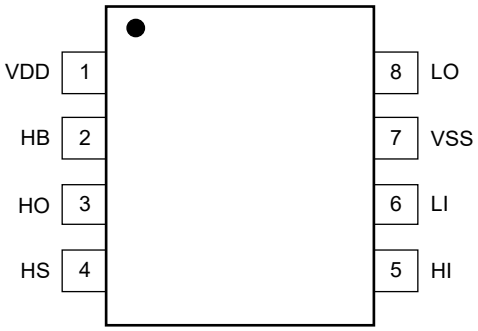
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

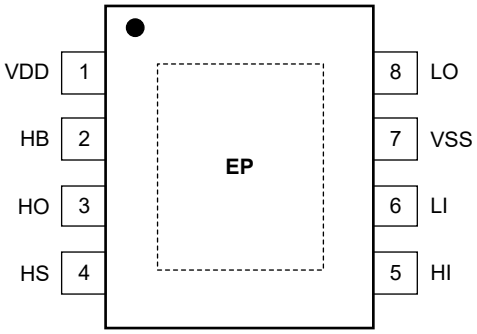
PIN CONFIGURATIONS

(TOP VIEW)



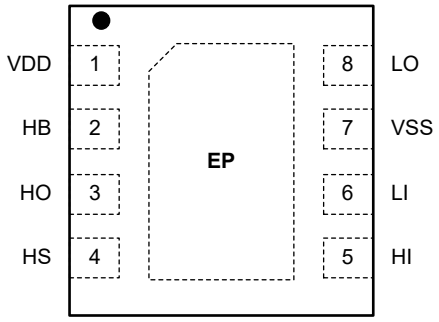
SOIC-8

(TOP VIEW)



SOIC-8 (Exposed Pad)

(TOP VIEW)



TDFN-4×4-8AL

PIN DESCRIPTION

PIN	NAME	I/O (1)	FUNCTION
1	VDD	P	Positive Supply of the Whole Driver. A decoupling capacitor in the range of 0.22μF to 4.7μF is connected between VDD and VSS pins. (2)
2	HB	P	High-side Bootstrap Supply. A bootstrap capacitor needs to be connected between HB and HS pins. The capacitor value varies with total gate charge of external MOSFET, the switching speed, as well as the voltage ripple criteria. Please refer to application information for detail.
3	HO	O	Output of the High-side Driver. Connect this pin to the gate of the high-side MOSFET.
4	HS	P	Reference Ground of the High-side Output Stage. Tie this pin directly to the source of external high-side power MOSFET.
5	HI	I	Input of the High-side Driver. (3)
6	LI	I	Input of the Low-side Driver. (3)
7	VSS	G	Reference Ground of the Device.
8	LO	O	Output of the Low-side Driver. Connect this pin to the gate of the low-side MOSFET.
Exposed Pad (4)	—	—	Thermal Pad. Connect directly to VSS with a large wide trace or polygon copper to achieve improved thermal conduction.

NOTES:

1. P: power supply, I: input, O: output, G: ground.
2. It is recommended to use the upper capacitance range for low temperature consideration.
3. Capacitors with typical value of 1nF to 10nF are recommended to be placed between HI/LI and VSS pins, which will be a great help to filter noise presented on these pins.
4. The exposed pad is internally connected to the substrate for thermal conduction and should be connected to the ground outside.

TYPICAL APPLICATION CIRCUIT

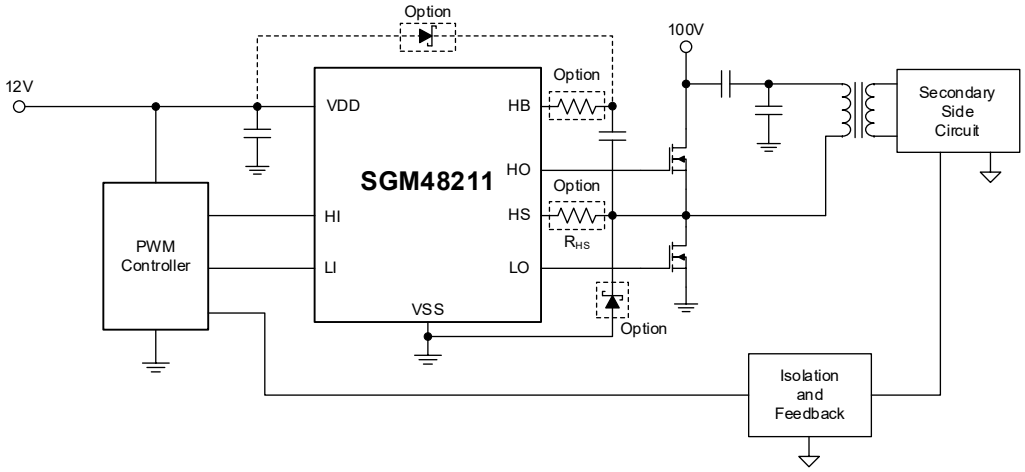


Figure 1. Typical Application Diagram

The capacitance value of the bootstrap capacitor is recommended to be no larger than 1μF to prevent excessive transient current breakdown of the bootstrap diode when charging the bootstrap capacitor.

If the Q_G of the power transistor is particularly large and requires a capacitance greater than 1μF, it is recommended to connect a resistor directly on the HB pin in series with the bootstrap capacitor to reduce the transient current. A 1Ω to 2Ω series resistor is recommended. It is important to note that this series resistance also increases the total turn-on resistance.

If it is not possible to increase the series resistor, it is recommended to add an external Schottky diode between the VDD and HB pins in parallel with the internal diode to share the transient current and reduce the effect of the transient current on the body diode. A Schottky diode like S115FP should be selected when $V_F \leq 0.8V$ @100mA.

A larger di/dt will generate a larger negative voltage on the HS pin. Adding a R_{HS} resistor can limit the peak of the negative voltage. If the negative voltage cannot be suppressed with the external R_{HS}, it is recommended to add a Schottky diode between HS and VSS to clamp the negative voltage. Connect the diode between HS pin and VSS pin directly as shown in Figure 1. Its minimum blocking voltage should be larger than the maximum positive voltage of the half bridge.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{HB} = 12V, V_{HS} = V_{SS} = 0V, no load on LO or HO, T_J = -40℃ to +140℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Currents						
VDD Quiescent Current	I_{DD}	V_{LI} = V_{HI} = 0V	0.08	0.13	0.2	mA
VDD Operating Current	I_{DDO}	f = 500kHz, C_{LOAD} = 0	0.2	1.25	2.3	mA
Boot Voltage Quiescent Current	I_{HB}	V_{LI} = V_{HI} = 0V	0.06	0.1	0.14	mA
Boot Voltage Operating Current	I_{HBO}	f = 500kHz, C_{LOAD} = 0	0.5	0.9	1.2	mA
HB to VSS Quiescent Current	I_{HBS}	V_{HS} = V_{HB} = 110V		14	45	μA
HB to VSS Operating Current	I_{HBSO}	f = 500kHz, C_{LOAD} = 0		0.43	0.8	mA
Input						
Input Voltage Threshold	V_{IH}		1.9	2.25	2.6	V
Input Voltage Threshold	V_{IL}		1.3	1.55	1.8	V
Input Voltage Hysteresis	V_{IHYS}			0.7		V
Input Pull-Down Resistance	R_{IN}			68		kΩ
Under-Voltage Lockout (UVLO)						
V_{DD} Turn-On Threshold	V_{DDR}		6.2	7	7.8	V
Hysteresis	V_{DDHYS}			0.5		V
V_{HB} Turn-On Threshold	V_{HBR}		5.2	6.4	7.6	V
Hysteresis	V_{HBHYS}			1		V
Bootstrap Diode						
Low-Current Forward Voltage	V_F	I_{VDD-HB} = 100μA		0.65	0.9	V
High-Current Forward Voltage	V_{FI}	I_{VDD-HB} = 100mA		0.95	1.2	V
Dynamic Resistance, $\Delta V_F/\Delta_I$	R_D	I_{VDD-HB} = 100mA and 80mA	0.5	0.9	1.5	Ω
LO Gate Driver						
Low Level Output Voltage	V_{OLL}	I_{LO} = 100mA	0.02	0.06	0.12	V
High Level Output Voltage	V_{OHL}	I_{LO} = -100mA, V_{OHL} = V_{DD} - V_{LO}	0.04	0.1	0.18	V
Peak Pull-Up Current	I_{OHL}	V_{LO} = 0V		4		A
Peak Pull-Down Current	I_{OLL}	V_{LO} = 12V		5		A
HO Gate Driver						
Low Level Output Voltage	V_{OLH}	I_{HO} = 100mA	0.02	0.06	0.12	V
High Level Output Voltage	V_{OHH}	I_{HO} = -100mA, V_{OHH} = V_{HB} - V_{HO}	0.04	0.1	0.18	V
Peak Pull-Up Current	I_{OHH}	V_{HO} = 0V		3.7		A
Peak Pull-Down Current	I_{OLH}	V_{HO} = 12V		4.6		A

SWITCHING CHARACTERISTICS

(V_{DD} = 12V, V_{HB} - V_{HS} = 12V, T_J = -40℃ to +140℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN (2)	TYP	MAX (2)	UNITS
Propagation Delays						
V_{LI} Falling to V_{LO} Falling	t_{DLFF}	C_{LOAD} = 0	18	28	42	ns
V_{HI} Falling to V_{HO} Falling	t_{DHFF}		18	28	42	ns
V_{LI} Rising to V_{LO} Rising	t_{DLRR}		18	31	47	ns
V_{HI} Rising to V_{HO} Rising	t_{DHRR}		18	31	47	ns
Delay Matching						
From HO Off to LO On	t_{MON}			3	10	ns
From LO Off to HO On	t_{MOFF}			3	10	ns
Output Rise and Fall Time						
LO Rise Time	t_R	C_{LOAD} = 1nF, from 10% to 90%		6.5	12	ns
HO Rise Time	t_R			6.5	12	ns
LO Fall Time	t_F	C_{LOAD} = 1nF, from 90% to 10%		4.5	7.5	ns
HO Fall Time	t_F			4.5	7.5	ns
LO	t_R	C_{LOAD} = 0.1μF, (3V to 9V)		235	365	ns
HO	t_R			235	365	ns
LO	t_F	C_{LOAD} = 0.1μF, (9V to 3V)		170	265	ns
HO	t_F			170	265	ns
Miscellaneous						
Minimum Input Pulse Width that Changes the Output (1)	t_{MIN}				33	ns

NOTES:

1. Ensure that the minimum pulse width of the input is greater than 33ns and configure enough dead time to prevent high-side and low-side transistor pass-through.
2. Specified by design and characterization, not production tested.

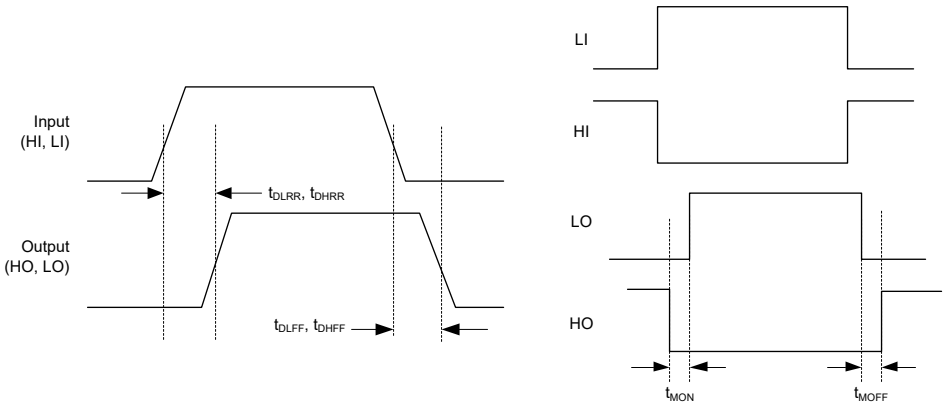
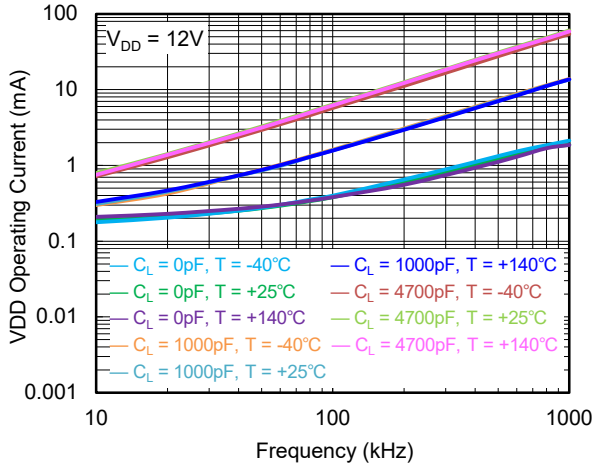


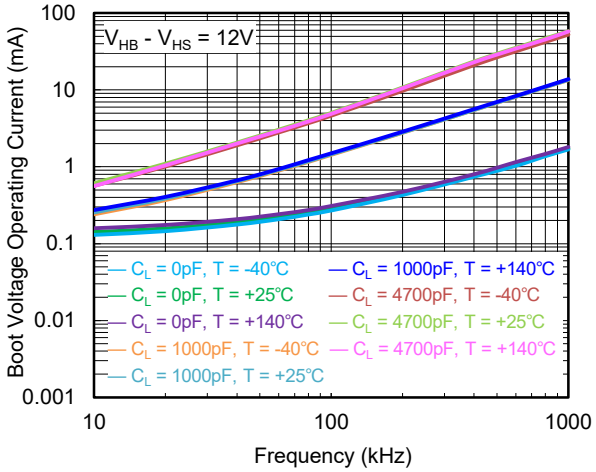
Figure 2. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

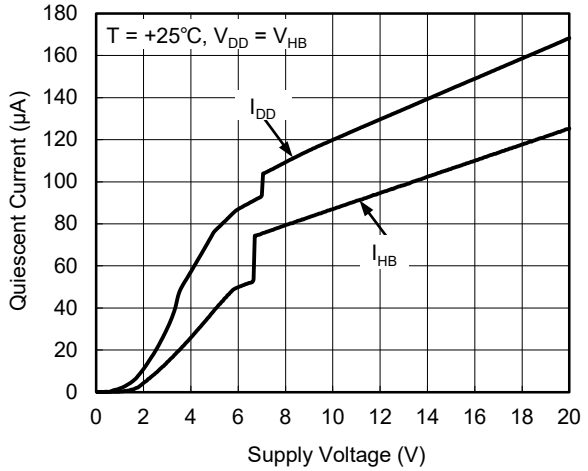
VDD Operating Current vs. Frequency



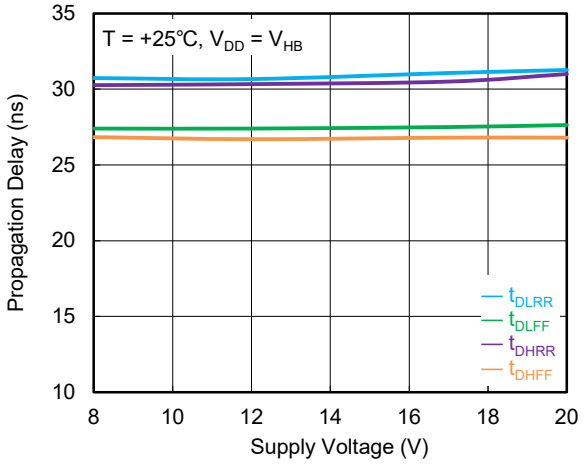
Boot Voltage Operating Current vs. Frequency (HB to HS)



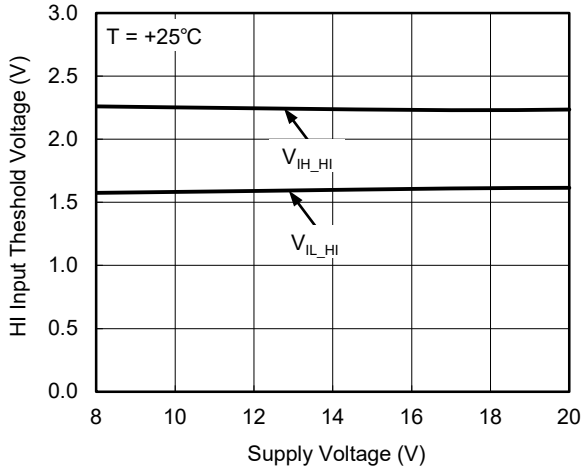
Quiescent Current vs. Supply Voltage



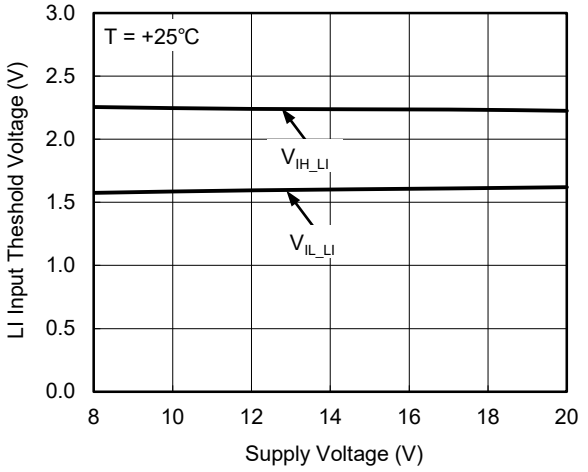
Propagation Delays vs. Supply Voltage



HI Input Threshold Voltage vs. Supply Voltage

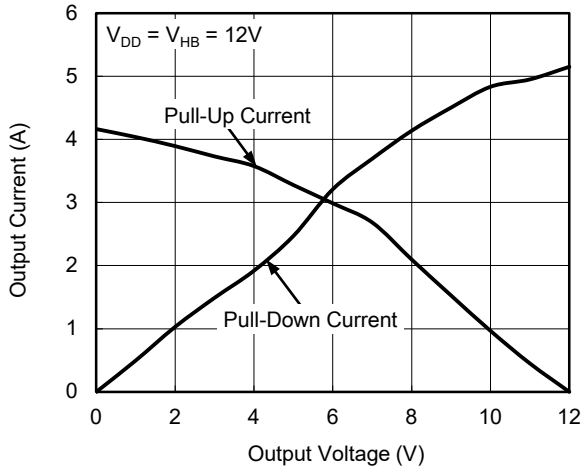


LI Input Threshold Voltage vs. Supply Voltage

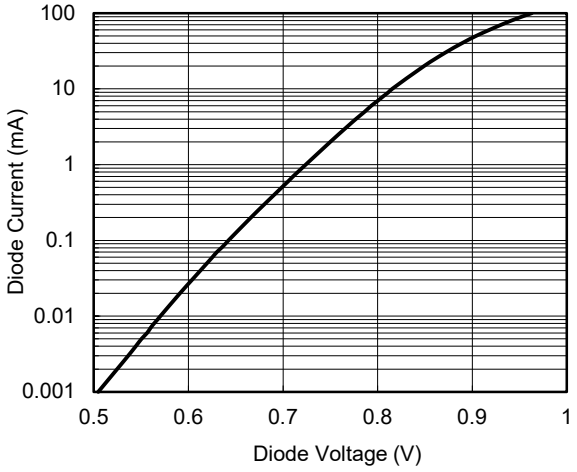


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

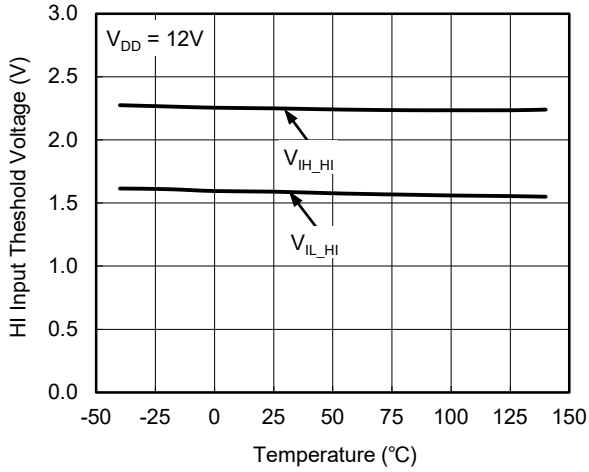
Output Current vs. Output Voltage



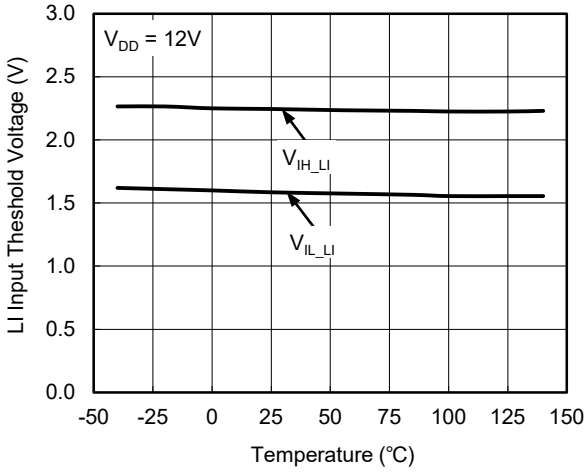
Diode Current vs. Diode Voltage



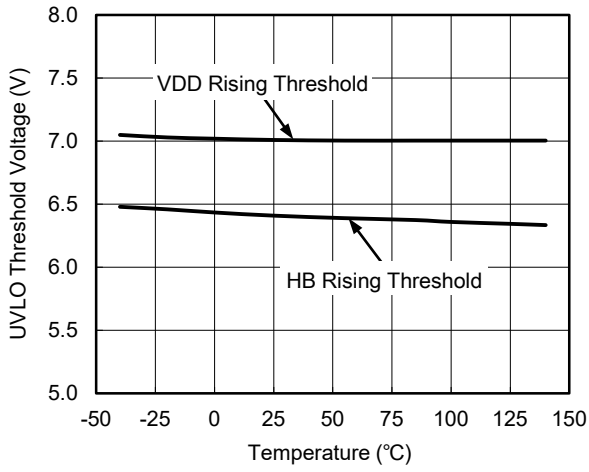
HI Input Threshold Voltage vs. Temperature



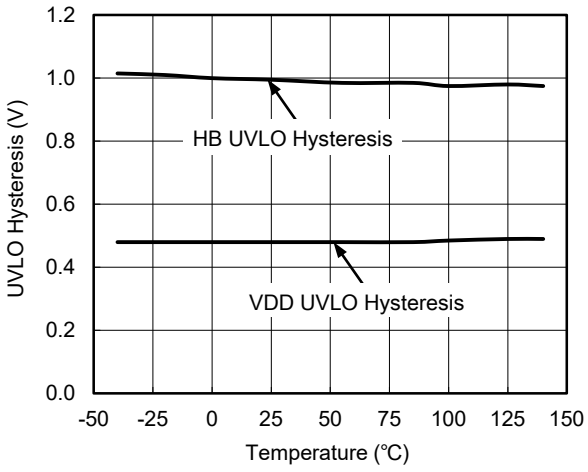
LI Input Threshold Voltage vs. Temperature



UVLO Threshold Voltage vs. Temperature

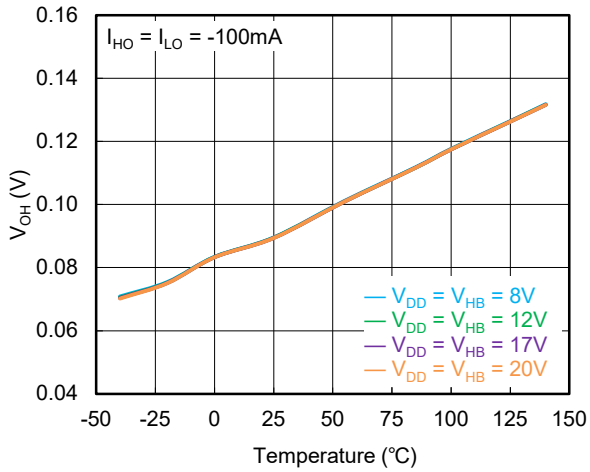


UVLO Hysteresis vs. Temperature

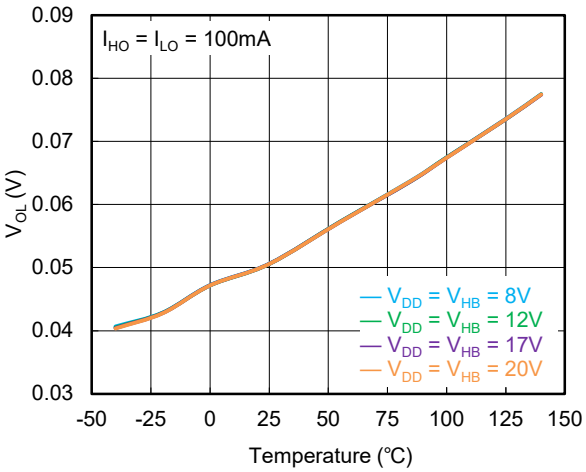


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

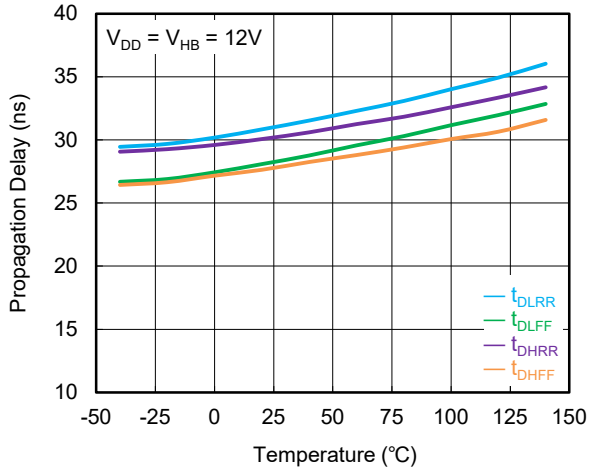
LO and HO High-Level Output Voltage vs. Temperature



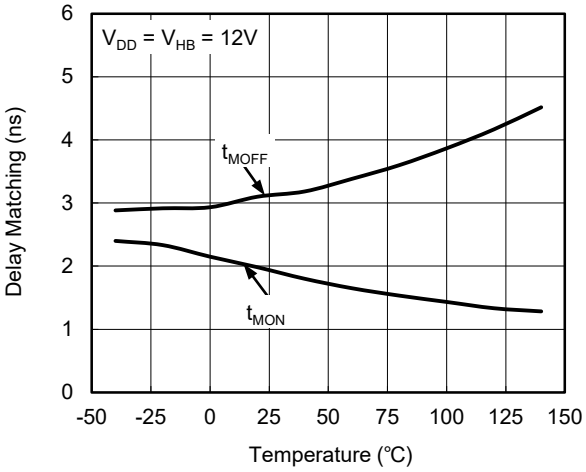
LO and HO Low-Level Output Voltage vs. Temperature



Propagation Delay vs. Temperature



Delay Matching vs. Temperature



FUNCTIONAL BLOCK DIAGRAM

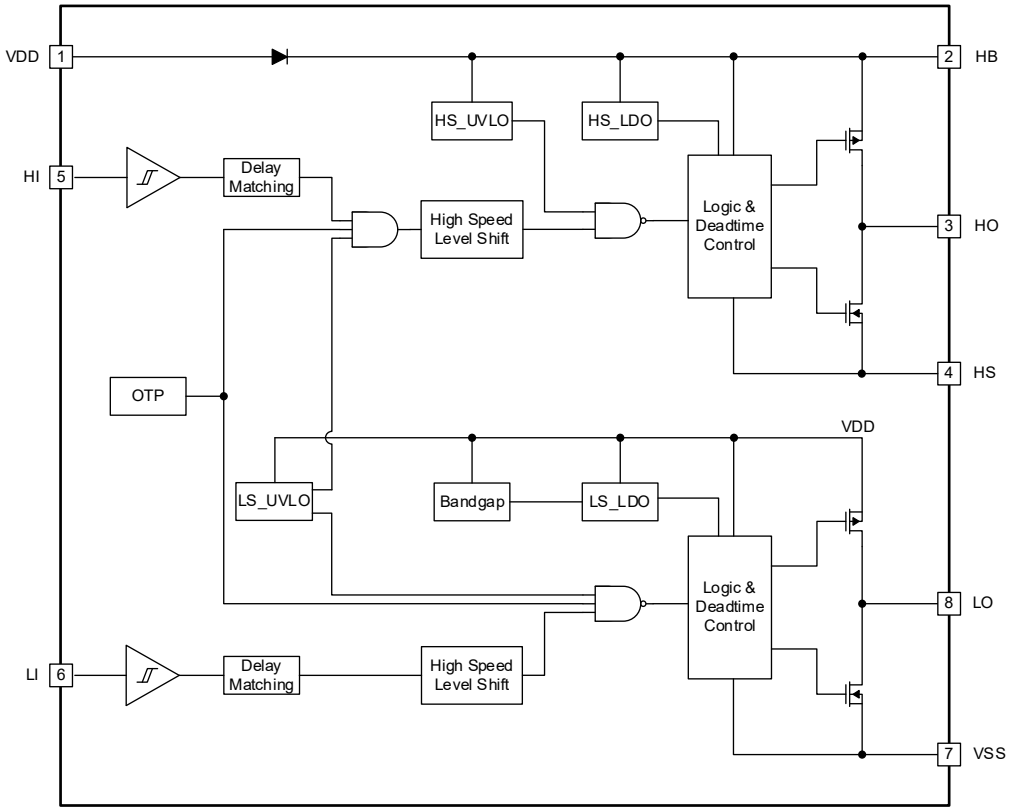


Figure 3. Functional Block Diagram

DETAILED DESCRIPTION

The SGM48211 is a high-side and low-side gate driver and is designed to drive two switches in a half-bridge configuration.

Highlights of the SGM48211 are listed in Table 1. Due to the combination of these features, the device can operate with high frequency and robustness.

Table 1. Prominent Features and Benefits

Feature	Benefit
4A peak source and sink current.	To drive large power MOSFET and minimum switching losses.
Wide input withstanding voltage range of -10V to 20V $V_{DC.}$	High robustness and reliability. Can be used in various applications.
120V internal bootstrap diode.	Large margin to meet telecom 100V surge requirements and reduce system cost.
Robust ESD circuitry.	Improved immunity to Common Mode (CM) and Differential Mode (DM) noises.
31ns (TYP) propagation delay.	Low current distortion.
3ns (TYP) delay matching between channels.	Better Symmetry of Positive and Negative waveform.
Both high-side and low-side drivers feature UVLO circuit.	Ensures two channels shutdown simultaneously.
CMOS/TTL optimized thresholds with wide voltage hysteresis.	Improved noise immunity.

Input Stage

The input of each channel is designed with 68kΩ input impedance (internal pull-down to VSS). The input stages of the SGM48211 are CMOS/TTL compatible and designed with 2.25V logic high and 1.55V logic low thresholds, 68kΩ equivalent input impedance. A 68kΩ pull-down resistor is integrated internally in each channel.

Output Stage

Both output stages of the two drivers are designed to source and sink 4A peak current. Thus it allows for driving MOSFETs with high current capability and low switching losses. VSS is the reference ground of the low-side output stage and HS is the reference ground of the high-side output stage.

Under-Voltage Lockout (UVLO)

UVLO protections are implemented in both bias supplies of the high-side and low-side drivers. Once triggered, the V_{DD} UVLO disables both drivers while the V_{HB} UVLO only disables the high-side driver. The rising UVLO thresholds of V_{DD} and V_{HB} are 7V with 0.5V hysteresis and 6.4V with 1V hysteresis respectively.

Level Shift

A level shift circuit is integrated to shift the input signal to the output stage of the high-side driver and provides the minimum delay matching with the low-side driver.

Bootstrap Diode

A 120V rated bootstrap diode is internally connected between VDD and HB pins of the SGM48211 for generating the high-side bias. During turn-on of the low-side MOSFET in each cycle, the capacitor connected between the HB and HS pins is charged from VDD to HS through the bootstrap diode which provides fast recovery time and low diode resistance for efficient operation.

Device Functional Modes

When the SGM48211 operates in normal mode (inactive UVLO), the outputs (HO and LO) of both drivers follow their corresponding input signals (HI and LI) as listed in Table 2.

Table 2. Device Logic Table

HI Pin	LI Pin	HO Pin (1)	LO Pin (2)
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H

NOTES:

1. With reference to HS.
2. With reference to VSS.

APPLICATION INFORMATION

The SGM48211 implements both the level-shifting and buffer-drive functions to boost the 3.3V signal to the gate-drive voltage to fully turn on the power device for achieving high-frequency switching, minimizing noise and controlling floating power-device gates and reducing power losses.

The SGM48211 is designed with low propagation delays and adopts low-inductance and compact package. It is available to drive wide band-gap power device such as GaN based switches for supporting very high switching frequency and low-cost component count.

Design Requirements

Table 3. Design Specifications

Design Parameter	Example Value
Supply Voltage, V_{DD}	12V
Voltage on HS, V_{HS}	0V to 100V
Voltage on HB, V_{HB}	12V to 112V
Output Current Rating, I_O	-4A to 4A
Operating Frequency	500kHz

Input Threshold Type

The SGM48211 can handle a maximum input voltage range from -10V to 20V to achieve enhanced robustness and allow compatibility with both inputs from microcontrollers, as well as higher-voltage inputs from gate-drive transformers. The inputs adopt TTL and CMOS compatible structure with a wide range of hysteresis. The voltage threshold is independent of V_{DD}.

Supply Voltage V_{DD}

The SGM48211 operates with a wide supply voltage range from 8V to 17V for applications such as driving Si MOSFETs, IGBTs, SiC MOSFETs and GaN FETs. The maximum voltage on VDD when applied to a single-ended power, and the differential voltage of the positive voltage and the negative voltage when applied to dual-railed power, as well as the bias supply voltage on the VDD pin should never exceed the values listed in the Absolute Maximum Ratings section.

Peak Driving Currents

The SGM48211 is designed with 4A peak source and sink currents for fast switching of power devices. For example, when the SGM48211 is used to drive an IPB60R120P7 power MOSFET with a DC bus voltage of 400V in a continuous conduction mode (CCM) PFC converter, the turn-on event and the turn-off event are supposed to be completed in approximately 14ns and 8ns (refer to DS of IPB60R120P7 with typical 36nC of total Q_G) separately. Therefore, a source current of 2.57A (= 36nC/14ns) and a sink current of 4.5A (= 36nC/8ns) or higher are necessary. The SGM48211 can provide 4A peak source current and sink currents larger than the requirements of IPB60R120P7.

In practical designs, the parasitic inductance of PCB traces will limit the di/dt of the gate driving current that may not reach the full peak current capability of the driver. To minimize this impact caused by the parasitic inductance, it is recommended to place the gate drive device as close to the power MOSFET as possible and design a tight gate driving loop with minimum parasitic inductance.

External gate resistors for turn-on and turn-off of the MOSFETs should be chosen carefully to achieve efficiency and EMI optimizations.

Propagation Delay

The SGM48211 features 31ns (TYP) propagation delay and 3ns (TYP) delay matching between the high-side and the low-side drivers, which makes it possible for the device to operate in very high frequency with little pulse distortion.

Power Dissipation

Power dissipation is the sum of conduction loss and switching loss as shown in Equation 1.

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

where P_{DC} is the conduction loss and can be calculated by Equation 2.

$$P_{DC} = I_Q \times V_{DD} \quad (2)$$

where

I_Q is the total quiescent current consumed by all internal block circuits and internal parasitic devices during switching (such as charging and discharging).

V_{DD} is the voltage between the VDD and VSS pins.

APPLICATION INFORMATION (continued)

P_G (P_{SW}) is the switching loss which can be calculated by Equation 3.

$$P_G = Q_G \times V_{DD} \times f_{SW} \quad (3)$$

where

f_{SW} is the switching frequency.

Q_G is the total gate charge of the MOSFET, typical 36nC of IPB60R120P7 in this example.

Half of P_G is dissipated during turn-on, and the other half is dissipated by both the external gate resistors and the internal resistance of the SGM48211 during turn-off.

When no external gate resistors are used, P_G is completely dissipated inside the device.

When using external gate resistors, the effective P_{G_PK} dissipated inside the package can be calculated by Equation 4.

$$P_{G_PK} = \frac{1}{2} \times P_G \times \left(\frac{R_{IN_ON}}{R_{IN_ON} + R_{EX_ON}} + \frac{R_{IN_OFF}}{R_{IN_OFF} + R_{EX_OFF}} \right) \quad (4)$$

where

R_{IN_ON} is the effective pull-up resistance of the output stage of SGM48211.

R_{EX_ON} is the total external turn-on resistance of gate resistor and internal gate resistance of the power MOSFET.

R_{IN_OFF} is the effective pull-down resistance of the output stage of SGM48211.

R_{EX_OFF} is the total external turn-off resistance of gate resistor and internal gate resistance of the power MOSFET.

Power Supply Recommendations

The SGM48211 operates in normal mode from the minimum 8V bias supply governed by the UVLO function to the maximum 17V bias supply limited by the 20V absolute maximum voltage with a 3V margin to allow for transient voltage spikes during switching.

UVLO functions are implemented in both V_{DD} and V_{HB} with a hysteresis function. The voltage thresholds of the UVLOs are typical 7V on V_{DD} - V_{SS} and 6.4V on V_{HB} - V_{HS} with respective 0.5V and 1V hysteresis.

To avoid from entering the UVLO mode caused by the voltage ripple lower than the hysteresis on both V_{DD} and V_{HB} during switching, local bypass capacitors must be placed between the VDD and VSS pins and between the HB and HS pins as close to the device as possible. Low-ESR, ceramic surface-mount capacitors with capacitance in the range of 0.22μF to 4.7μF between VDD and VSS pins and 0.022μF to 0.1μF between HB and HS pins are recommended.

Layout Guidelines

The following layout recommendations should be considered:

• Place the SGM48211 as close to the MOSFETs as possible.

• Locate the bootstrap capacitor (V_{HB} - V_{HS}) and decoupling capacitor (V_{DD} - V_{SS}) as close to the device as possible.

• Minimize the gate drive loops from the output pins to the gate of MOSFETs. Tie the HS and VSS pins directly to the corresponding source of MOSFETs in short distance.

• Exposed pad should be connected to VSS net and with large polygon copper for improved thermal conduction.

• VDD traces should be away from the high-side pins and the LO pin.

• A minimum width of 60mils is recommended for the HO and LO traces.

• Two or more vias should be used if routing through different layers and for thermal conduction on VSS net.

• Input traces of HI and LI should be away from traces with higher dV/dt.

Thermal Considerations

Measures that reduce the effective thermal resistances from the package to PCB or to the open air should be taken to keep the junction temperature within rated limits.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

SEPTEMBER 2024 – REV.A.3 to REV.A.4	Page
Changed Pin Description section	4
Changed Typical Application Circuit section	5

MAY 2024 – REV.A.2 to REV.A.3	Page
Added Typical Application Circuit section	5

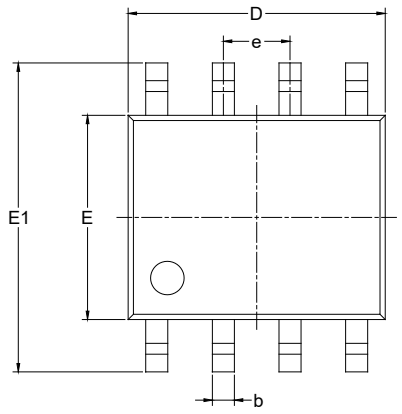
APRIL 2024 – REV.A.1 to REV.A.2	Page
Added Absolute Maximum Ratings section	2
Changed Typical Performance Characteristics section	9

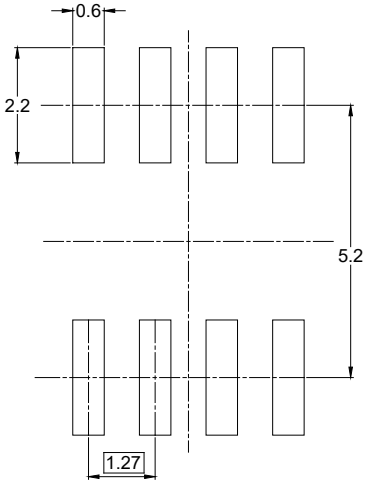
JANUARY 2024 – REV.A to REV.A.1	Page
Added Pin Description section	4
Added and Changed Switching Characteristics section	7
Changed Application Information section	14

Changes from Original (DECEMBER 2023) to REV.A	Page
Changed from product preview to production data	All

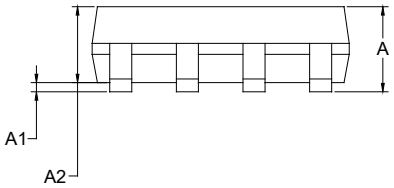
PACKAGE OUTLINE DIMENSIONS

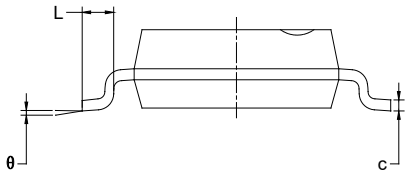
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)



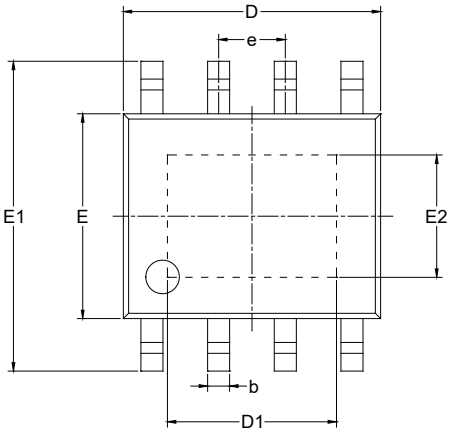


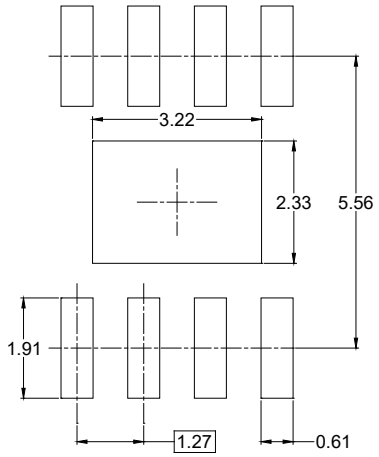
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

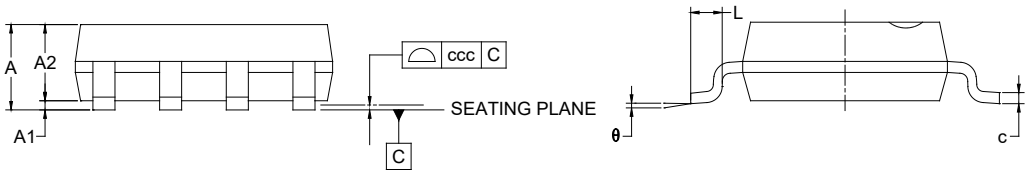
PACKAGE OUTLINE DIMENSIONS

SOIC-8 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)

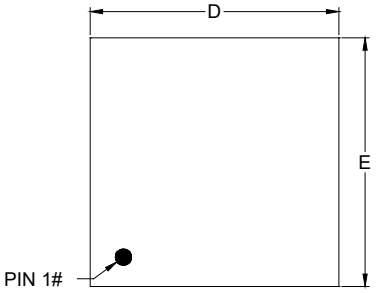


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A			1.700
A1	0.000	-	0.150
A2	1.250	-	1.650
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
D1	3.020	-	3.420
E	3.800	-	4.000
E1	5.800	-	6.200
E2	2.130	-	2.530
e	1.27 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

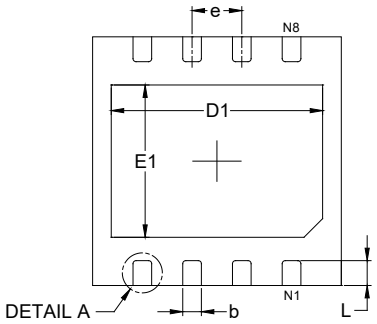
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

PACKAGE OUTLINE DIMENSIONS

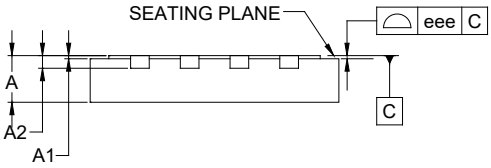
TDFN-4×4-8AL



TOP VIEW

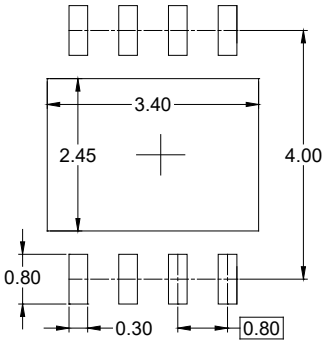


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



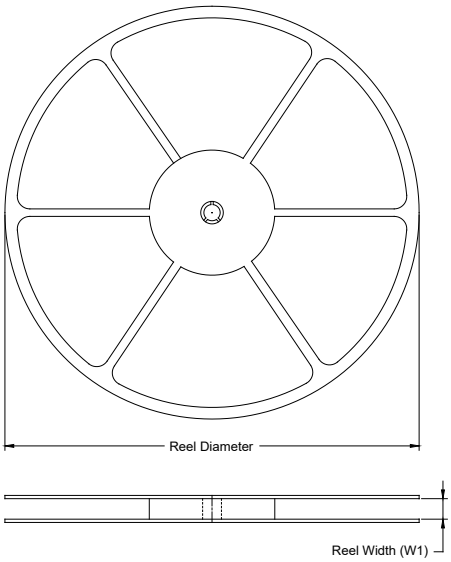
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.250	-	0.350
D	3.900	-	4.100
E	3.900	-	4.100
D1	3.300	-	3.500
E1	2.350	-	2.550
e	0.800 BSC		
L	0.300	-	0.500
eee	0.080		

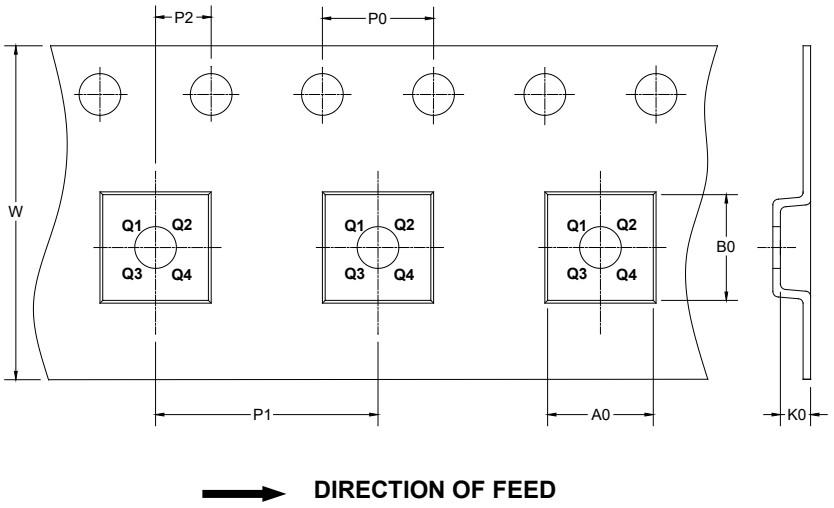
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



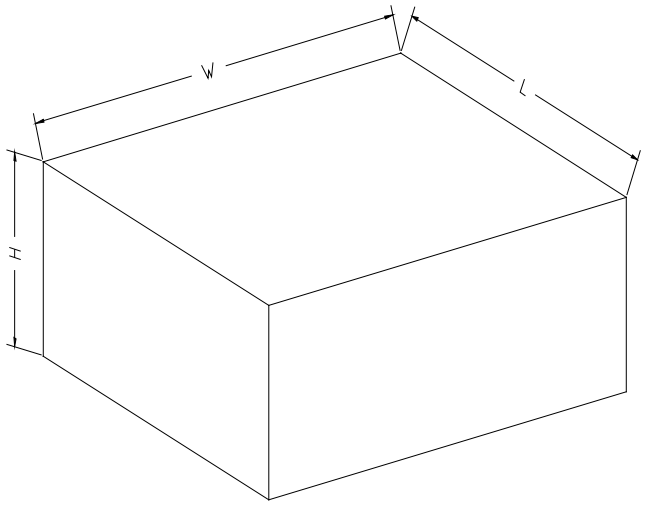
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
SOIC-8 (Exposed Pad)	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
TDFN-4×4-8AL	13"	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002