SGM37604S
High Efficiency 4-String White LED Driver

GENERAL DESCRIPTION

The SGM37604S is a high efficiency 4-string white LED driver with an integrated 1.2MHz Boost converter. The SGM37604S operates from 3V to 5.5V input range, and is capable of driving up to 9 LEDs in series for 25mA maximum LED current per string while achieving high conversion efficiency. An adaptively current-regulated method allows different LED string voltages while LED current remains in regulation. The LED current is programmed through an I^2C interface or a PWM signal input. These features make it optimized for compact solutions and ideal for LCD display backlighting.

The SGM37604S is available in a Green WLCSP-1.35×1.7-12B package. It operates over the -40℃ to +85℃ temperature range.

APPLICATIONS

Power Source for Smart Phone and Tablet Backlighting

FEATURES

- **2% Matched Current Sinks across Process, Voltage and Temperature**
- **0.5% Current Sink Accuracy across Process, Voltage and Temperature**
- **12-Bit Resolution for Dimming Control**
- **Up to 91% Boost Efficiency**
- **Support 1 to 4 LED Strings in Parallel at Maximum 29.5V Output**
- **PWM Dimming Interface**
- **Programmable I^2C Interface**
- **Phase Shift Function**
- **Hybrid PWM + Current Dimming for Higher LED Driver Optical Efficiency**
- **1.2MHz Switching Frequency**
- **Low EMI by Conducting Ringing Cancelling**
- **Protection Features**
  - **Over-Voltage Protection**
  - **Over-Current Protection**
  - **Thermal Shutdown**

TYPICAL APPLICATION

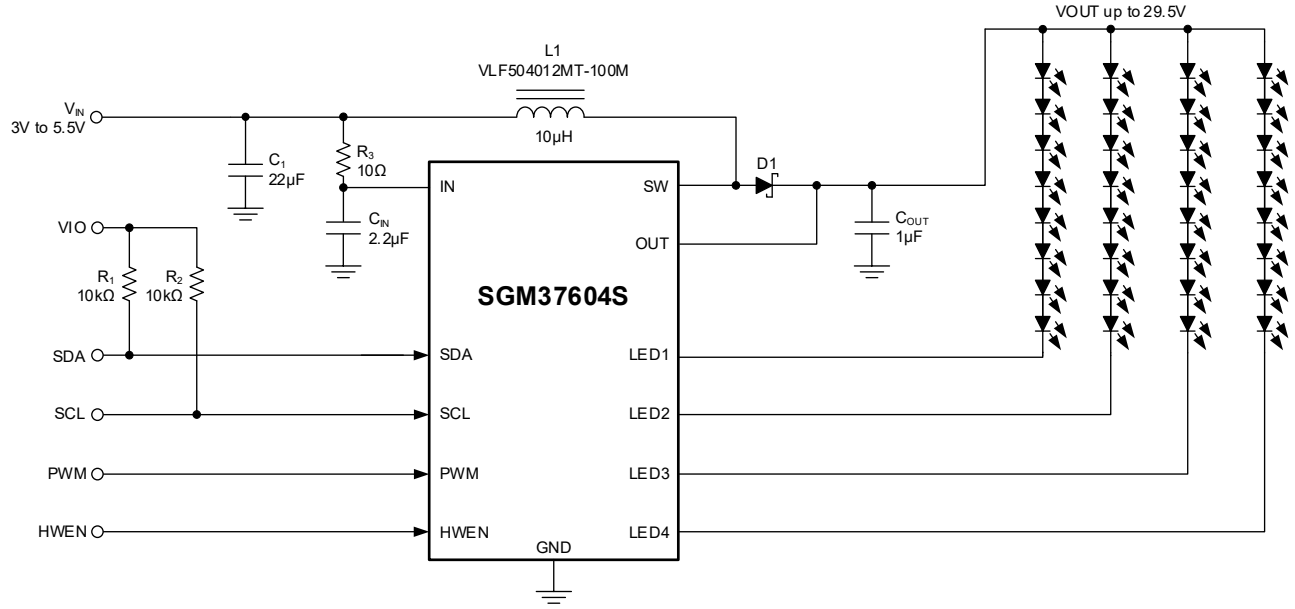


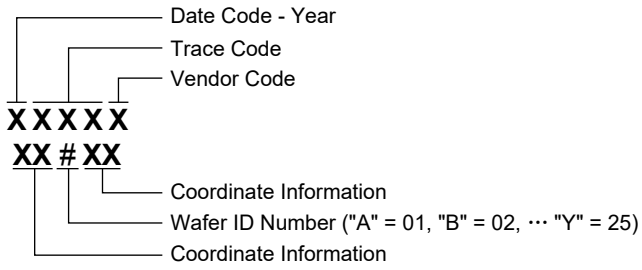
Figure 1. Typical Application

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM37604S	WLCSP-1.35×1.7-12B	-40℃ to +85℃	SGM37604SYG/TR	0D9 XXXXX XX#XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN ..... -0.3V to 6V
OUT ..... -0.3V to 33V
SW ..... -0.3V to 33V
LED1, LED2, LED3, LED4 ..... -0.3V to 33V
HWEN, PWM, SDA, SCL ..... -0.3V to 6V
Package Thermal Resistance
WLCSP-1.35×1.7-12B, θ_{JA} ..... 91℃/W
WLCSP-1.35×1.7-12B, θ_{JB} ..... 28.3℃/W
WLCSP-1.35×1.7-12B, θ_{JC} ..... 42℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 1000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

IN ..... 3V to 5.5V
HWEN, PWM, SDA, SCL ..... 0V to 5.5V
Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

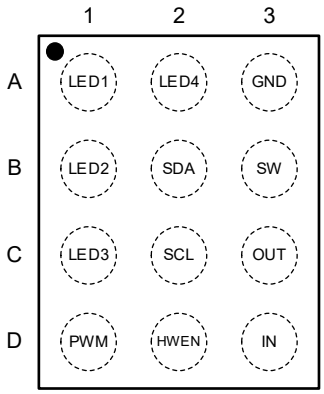
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

SGM37604S (TOP VIEW)



WLCSP-1.35×1.7-12B

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
A1	LED1	I	Current Sink Regulation Input. The Boost loop regulates the lowest V_{HR} to 200mV.
A2	LED4	I	Current Sink Regulation Input. The Boost loop regulates the lowest V_{HR} to 200mV.
A3	GND	O	Ground Pin.
B1	LED2	I	Current Sink Regulation Input. The Boost loop regulates the lowest V_{HR} to 200mV.
B2	SDA	I/O	I^2C Data Signal.
B3	SW	I	Drain Connection for Internal Low-side N-Channel MOSFET. Connect to the anode of an external Schottky diode.
C1	LED3	I	Current Sink Regulation Input. The Boost loop regulates the lowest V_{HR} to 200mV.
C2	SCL	I	I^2C Clock Signal.
C3	OUT	I	Output Voltage Sense Pin. It is used for sensing the output voltage for over-voltage protection. Connect to the positive terminal of the output capacitor.
D1	PWM	I	PWM Dimming Signal Input.
D2	HWEN	I	Hardware Enable Input Pin. Drive HWEN high to enable the device and allow I^2C write commands or PWM control.
D3	IN	I	Input Supply Pin. Connect a at least 2.2μF bypass capacitor from IN to GND.

NOTE: I: input, O: output, I/O: input or output.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, T_A = -40℃ to +85℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Boost						
LED Current Matching I_{LED1} to I_{LED2} to I_{LED3} to I_{LED4}	I_{MATCH} (1)	I_{LED} = 25mA, T_A = +25℃	-2.5	0.25	2.5	%
		I_{LED} = 12.21μA, T_A = +25℃	-8	2	8	
Absolute Accuracy (I_{LED1}, I_{LED2}, I_{LED3}, I_{LED4})		I_{LED} = 25mA, T_A = +25℃	-3.5	0.1	3.5	%
		I_{LED} = 12.21μA, T_A = +25℃	-10	0.5	10	
Minimum LED Current (per String)	I_{LED_MIN}			12.21		μA
Maximum LED Current (per String)	I_{LED_MAX}			25		mA
Regulated Current Sink Headroom Voltage	V_{HR}	I_{LED} = 25mA		200		mV
NMOS Switch On-Resistance	R_{NMOS}	I_{SW} = 250mA		0.18	0.35	Ω
NMOS Switch Current Limit	I_{CL}	T_A = +25℃	1.95	2.35	2.70	A
Output Over-Voltage Protection	V_{OVP}		28	29.5	31	V
OVP Hysteresis	V_{OVP_HYS}			3		V
Switching Frequency	f_{SW}		950	1200	1450	kHz
Maximum Boost Duty Cycle	D_{MAX}		89	93		%
Shutdown Current	I_{SHDN}	Chip enable bit = 0, SDA = SCL = IN or GND		0.1		μA
Thermal Shutdown	T_{SD}			155		℃
Thermal Shutdown Hysteresis				25		
PWM Input						
PWM Dimming Frequency Range	DFR		20		100	kHz
Turn-On Delay from Shutdown to Backlight On	$t_{START-UP}$	PWM input active, PWM = logic high, HWEN input from low to high, f_{PWM} = 20kHz (50% duty cycle)		8.5		ms
Input Logic High	V_{IH}	HWEN, SCL, SDA, PWM inputs	1.4			V
Input Logic Low	V_{IL}	HWEN, SCL, SDA, PWM inputs			0.4	

NOTE:
1. LED current matching depends on the two channels with the largest current difference, and its calculation formula is (I_{LED_MAX} - I_{LED_MIN})/(I_{LED_MAX} + I_{LED_MIN}) × 100%.

I²C TIMING REQUIREMENTS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCL Clock Period	t_1	2.5			μs
Data in Setup Time to SCL High	t_2	100			ns
Data Out Stable after SCL Low	t_3	0			ns
SDA Low Setup Time to SCL Low (Start)	t_4	100			ns
SDA High Hold Time after SCL High (Stop)	t_5	100			ns

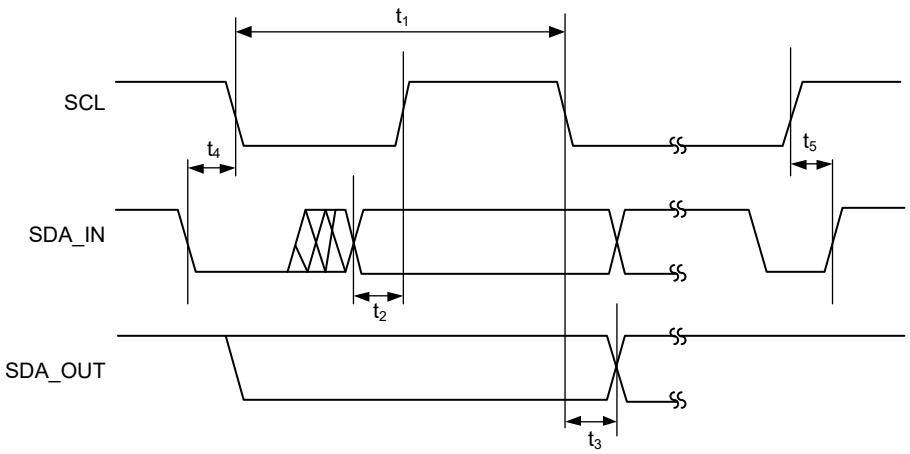


Figure 2. I²C Timing

FUNCTIONAL BLOCK DIAGRAM

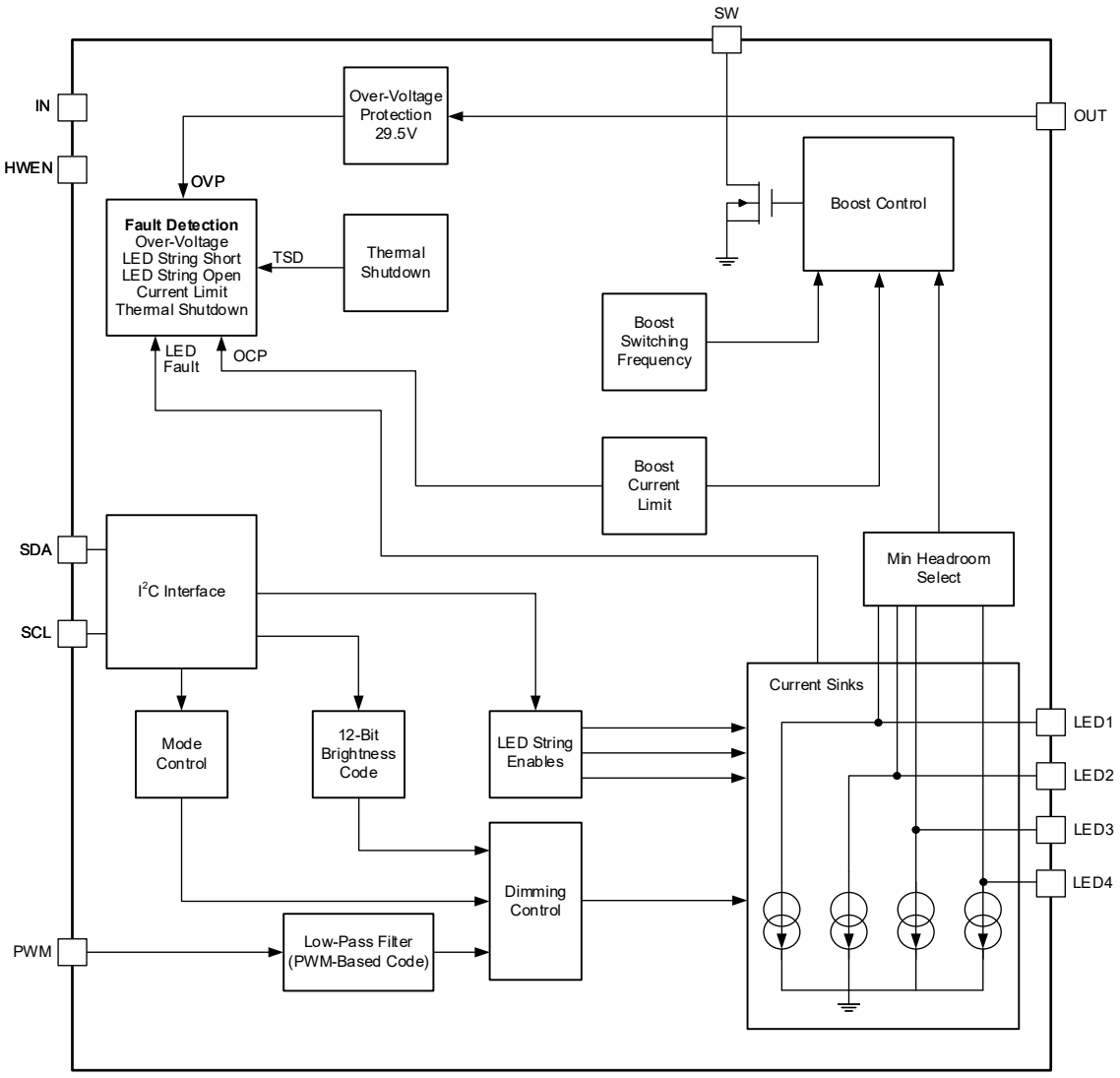
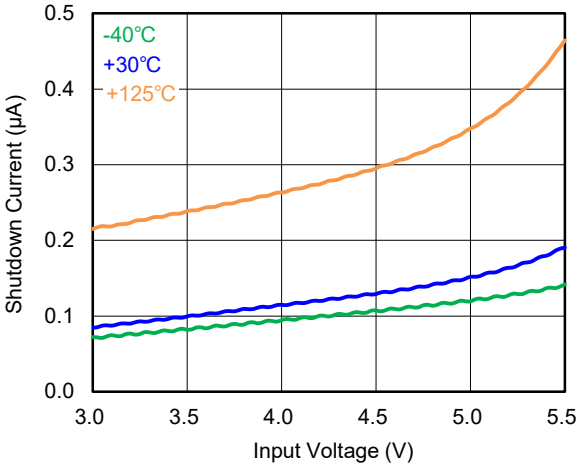


Figure 3. Functional Block Diagram

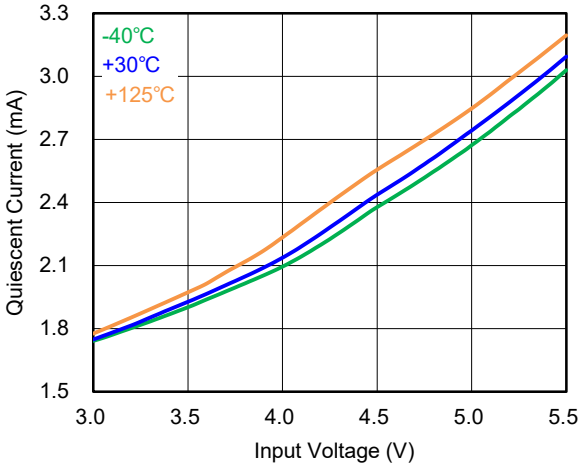
TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = +25℃, V_{IN} = 3.7V, L1 = 10μH (LVS505020-100M-NEY), D1 = PMEG4010EH, unless otherwise noted.

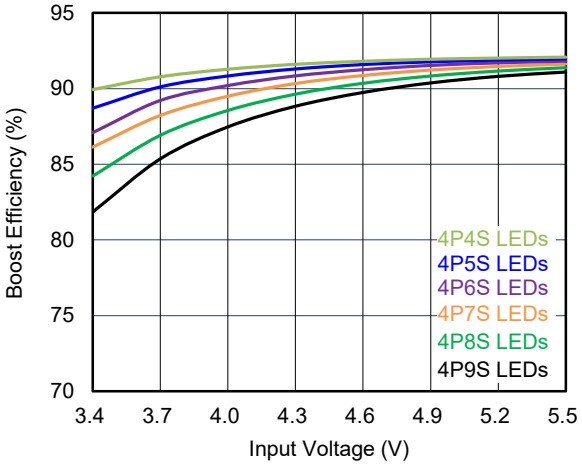
Shutdown Current vs. Input Voltage



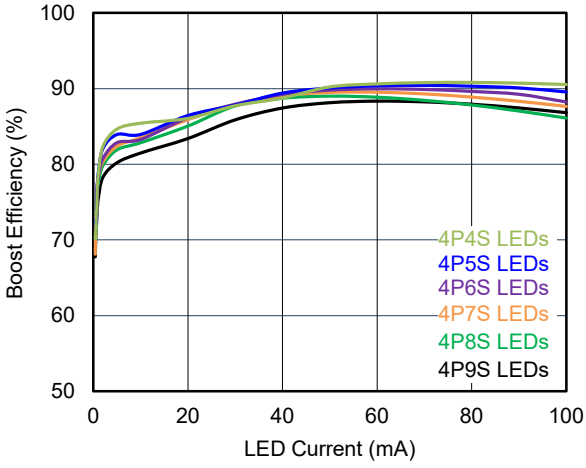
Quiescent Current (Switching) vs. Input Voltage



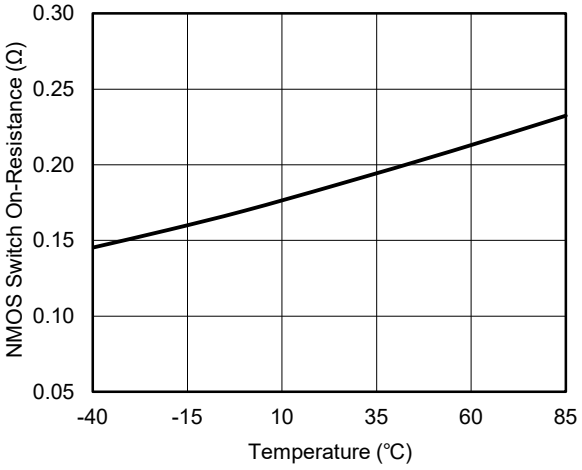
Boost Efficiency vs. Input Voltage



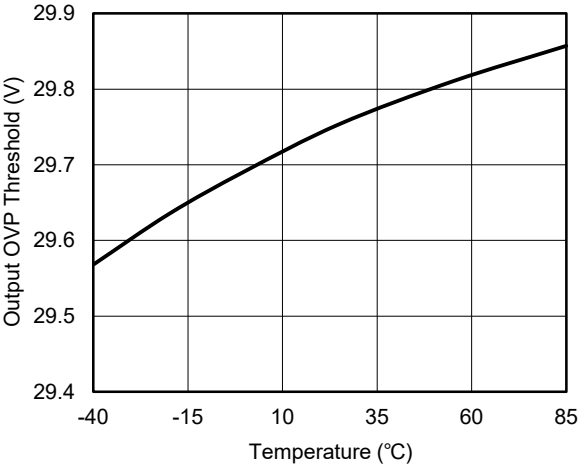
Boost Efficiency vs. LED Current



NMOS Switch On-Resistance vs. Temperature



Output Over-Voltage Protection Threshold vs. Temperature



REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

I^2C Slave Address of SGM37604S is: 0x36 (0b0110110 + R/W)

ADDRESS	REGISTER NAME	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x00	Device Code	DEV_COD[7:0]							
0x01	Software Reset	Reserved							SOFT_RST
0x10	Enable Control	Reserved			LED4_EN	LED3_EN	LED2_EN	LED1_EN	DEV_EN
0x11	Brightness Control	Reserved	LED_MOD[1:0]		RAMP_EN	Reserved			
0x1A	Brightness Code 0	Reserved				BRT_COD[3:0]			
0x19	Brightness Code 1	BRT_COD[11:4]							
0x1F	Fault Information	Reserved			SO_FLAG	SC_FLAG	TSD_FLAG	OC_FLAG	OVP_FLAG

Bit Types:
R: Read only
R/W: Read/Write

REG0x00: Device Code Register [Reset = 0x41]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	DEV_COD[7:0]	01000001	R	Reserved

REG0x01: Software Reset Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:1]	Reserved	0000000	R	Reserved
D[0]	SOFT_RST	0	R/W	Software Reset 0 = Normal Operation (default) 1 = Reset the device. It will return 0 automatically.

REG0x10: Enable Control Register [Reset = 0x1F]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	Reserved	000	R	Reserved
D[4]	LED4_EN	1	R/W	LED4 Enable 0 = Disabled 1 = Enabled (default)
D[3]	LED3_EN	1	R/W	LED3 Enable 0 = Disabled 1 = Enabled (default)
D[2]	LED2_EN	1	R/W	LED2 Enable 0 = Disabled 1 = Enabled (default)
D[1]	LED1_EN	1	R/W	LED1 Enable 0 = Disabled 1 = Enabled (default)
D[0]	DEV_EN	1	R/W	Device Enable 0 = Disabled 1 = Enabled (default)

REGISTER MAP (continued)

REG0x11: Brightness Control Register [Reset = 0x65]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R	Reserved
D[6:5]	LED_MOD[1:0]	11	R/W	00 = I^2C Only 01 = PWM Only 10 = I^2C × PWM 11 = I^2C × PWM (default)
D[4]	RAMP_EN	0	R/W	Ramp Enable 0 = Disabled (default) 1 = Enabled
D[3:0]	Reserved	0101	R	Reserved

REG0x1A: Brightness Code 0 Register [Reset = 0xFF]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	1111	R	Reserved
D[3:0]	BRT_COD[3:0]	1111	R/W	Lower 4 Bits of the 12-Bit Brightness Code

REG0x19: Brightness Code 1 Register [Reset = 0xFF]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	BRT_COD[11:4]	11111111	R/W	High Byte of the 12-Bit Brightness Code

REG0x1F: Fault Information Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	Reserved	000	R	Reserved
D[4]	SO_FLAG	0	R	LED String Open Fault Flag 0 = No LED Open Fault (default) 1 = LED Open Fault
D[3]	SC_FLAG	0	R	Short-Circuit Fault Flag 0 = No short-circuit fault (default) 1 = Short-circuit fault
D[2]	TSD_FLAG	0	R	Thermal Shutdown Fault Flag 0 = No thermal shutdown fault (default) 1 = Thermal shutdown fault
D[1]	OC_FLAG	0	R	Current Limit Fault Flag 0 = No current limit fault (default) 1 = Current limit fault
D[0]	OVP_FLAG	0	R	Output Over-Voltage Fault Flag 0 = No over-voltage fault (default) 1 = Over-voltage fault

DETAILED DESCRIPTION

The SGM37604S is an LED driver that powers the backlight of the display screen. It can support up to 4 LED backlight channels, and each channel can support up to 25mA of sink current. The device supports three different dimming methods: configuring the internal register via I^2C interface, changing the duty cycle of external PWM input, or combining the PWM dimming and I^2C dimming.

Enable the SGM37604S

The SGM37604S can be enabled by setting HWEN to logic high. Conversely, the SGM37604S can be disabled by setting HWEN to logic low. When the device is disabled, the device goes into shutdown mode, and the Boost converter and current sink terminate operation, in addition, the register will be reset to the default value.

Enable the Current Sink

By default, all current channels of the SGM37604S are enabled. The enable status of each current sink can be controlled through the register, which allows the device to adapt to different LED configurations.

Figure 4 and Figure 5 depict the timing diagrams for enabling the current sink via PWM or I^2C. When the enable bit of the current channel inside the device is set to 1, the device enters the standby state and waits for the non-zero PWM input. When the device detects a non-zero PWM input, it converts the PWM input into a brightness dimming code for LED dimming. In applications where I^2C function is not used, the LED brightness of the SGM37604S can be adjusted by changing the PWM duty cycle.

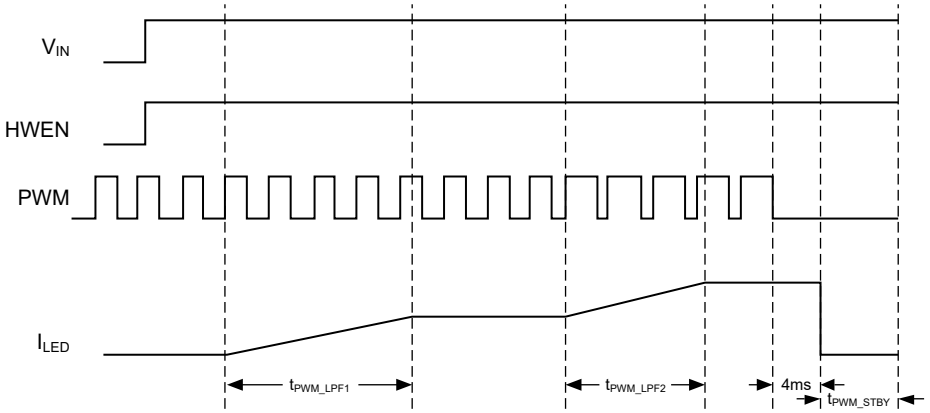


Figure 4. Enabling the Current Sink with PWM

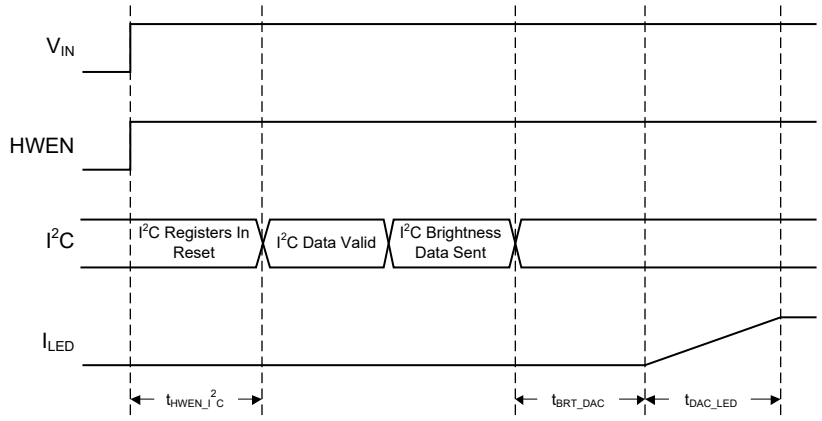


Figure 5. Enabling the Current Sink with I^2C

DETAILED DESCRIPTION (continued)

SGM37604S Start-Up

Table 1 shows the operating status of the SGM37604S in different configurations. When HWEN is high, the device exits the shutdown state. When the PWM is continuously low or the brightness code in the register is zero, the current sink is disabled and the device is in standby mode.

Regulated Headroom Voltage

Due to the nonlinear differences of LED's forward voltage, the SGM37604S needs to ensure that the LED string in each channel can reach the specified LED current. If LED4 is enabled to achieve the specified LED current corresponding to the anode voltage that is higher than the other three channels, the SGM37604S will use the LED4 channel as the feedback adjustment point of the Boost converter, and the cathode voltage of LED4 is set as V_{HR}.

Table 1. SGM37604S Operating Modes

Device Enable DEV_EN Bit	LED Enable LED1_EN & LED2_EN & LED3_EN & LED4_EN Bits	PWM Input	I²C Brightness Code BRT_COD[11:0]	Brightness Mode LED_MOD[1:0]	LED Current
0	XXXX	X	XXX	XX	Off, device disabled
1	0000	X	XXX	XX	Boost enabled, LED current disabled
1	At least one enabled	X	000	00	Off, device in standby mode
1	At least one enabled	X	Code > 000	00	See (1)
1	At least one enabled	0	XXX	01	Off, device in standby mode
1	At least one enabled	PWM Signal	XXX (2)	01	See (1)
1	At least one enabled	0	XXX	10 or 11	Off, device in standby mode
1	At least one enabled	X	000	10 or 11	Off, device in standby mode
1	At least one enabled	PWM Signal	Code > 000	10 or 11	See (1)

NOTES:

1. I_{LED} is calculated by the equations from Equation 1 to Equation 8 below in Brightness Control Modes.
2. Code is forbidden to set to 0.

Brightness Control Modes

The SGM37604S has 3 brightness control modes:

1. I^2C Only (brightness mode 00)
2. PWM Only (brightness mode 01)
3. I^2C × PWM (brightness mode 10 or 11)

I^2C Only (Brightness Mode 00)

In brightness control mode 00, only the I^2C Brightness registers control the LED current. The brightness data (BRT) consists of the two brightness registers (4 LSBs) and (8 MSBs) (REG0x1A[3:0] and REG0x19[7:0], respectively). The LED current only changes when the MSBs are written, which means that to do a full 12-bit current change via I^2C, first the 4 LSBs of REG0x1A are written and then the 8 MSBs of REG0x19 are written.

The 12-bit code (0 to 4095) is in control of the LED current as follows:

DETAILED DESCRIPTION (continued)

When the code is from 256 to 4095, the average LED current increases proportionally to the brightness code and follows the below relationship (see Figure 7).

When the code is an odd integer,

$$I_{LED\_AVG} = 12.21\mu A \times 0.5 \times (code - 1) \quad (1)$$

When the code is an even integer,

$$I_{LED\_AVG} = 12.21\mu A \times 0.5 \times code \quad (2)$$

where

I_{LED_AVG} = average LED current

When the code is from 16 to 255, the average LED current is calculated by Equation 1 and Equation 2 and the LED current is in current-to-PWM control (see Figure 7) with a constant maximum current, while the duty cycle changes following the code.

When the code is from 1 to 15, the average LED current increases exponentially to the brightness code, and follows the relationship by Equation 3 (see Figure 7). The LED current is also in current-to-PWM control, the duty cycle is 16/256 constantly, and the amplitude of current pulse is 16 times of its corresponding average current.

$$I_{LED\_AVG} = 12.21\mu A \times 1.149^{(code - 1)} \quad (3)$$

Code 1 programs the LED current to 12.21μA with 25mA maximum LED current. Code 0 programs 0 current.

When bit[4] is set to 1 in REG0x11, ramp function is enabled. Then when bits[7:4] in REG0x19 are not all 0 (codes from 256 to 4095), the ramp rate is 128μs/step. When bits[7:4] in REG0x19 are all 0 (codes from 1 to 255), the ramp rate is 1024μs/step. For example, if the code is set from 2000 to 4001, I_{LED_AVG} will change from 12.21mA to 24.42mA, the corresponding ramp rate = 128μs/step, so the ramp time for I_{LED_AVG} = [(4001 - 1) × 0.5 - 2000 × 0.5] × 128μs = 128ms.

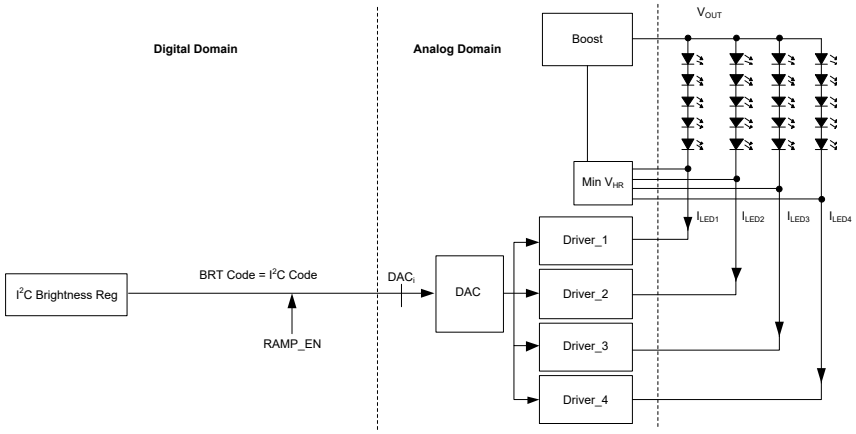


Figure 6. Brightness Control 00 (I^2C Only)

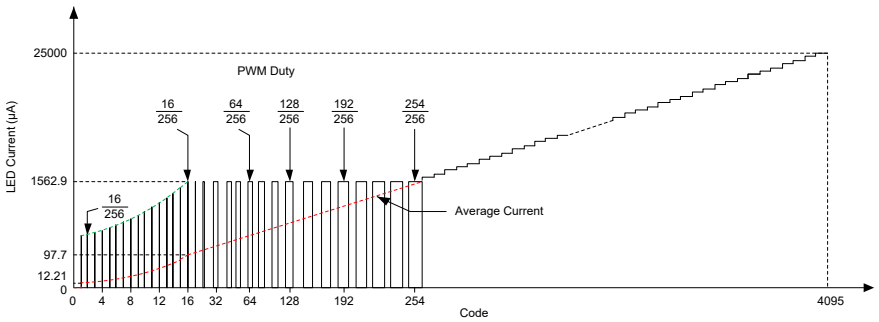


Figure 7. LED Current vs. Brightness Code (Mode 00)

DETAILED DESCRIPTION (continued)

PWM Only (Brightness Mode 01)

In brightness mode 01, only the PWM input sets the brightness. The I^2C code is ignored and forbidden to set to 0. The LED current is proportional with the PWM duty cycle and the maximum LED current is 25mA.

When the PWM pin is constantly high, the V_{REF} voltage is regulated to 2048mV typically. When the duty cycle of the input PWM signal is low, the regulation voltage is reduced, and the LED current is reduced. Therefore, it achieves LED brightness dimming. The relationship between the duty cycle and V_{REF} regulation voltage is given by Equation 4:

$$V_{REF} = Duty \times 2048mV \quad (4)$$

where

Duty = duty cycle of the PWM signal

2048mV = internal reference voltage

Then the value of V_{REF} is the PWM-based code for brightness dimming. The LED current increases proportionally to the brightness code and follows the relationship (see Figure 10):

$$I_{LED\_AVG} = 12.21\mu A \times code \quad (5)$$

This is valid from codes 1 to 2048. Code 0 programs 0 current. When the code < 16, the LED current is in current-to-PWM control. The duty cycle of the PWM is 1/8, and the amplitude of current pulse is 8 times of its corresponding average current. Figure 10 (a) shows the zoomed graph from codes 0 to 16 in Figure 10. There is no ramp function in this mode.

Thus, the user can easily control the WLED brightness by controlling the duty cycle of the PWM signal. The PWM frequency is in the range from 20kHz to 100kHz.

As shown in Figure 8, the IC chops up the internal 2048mV reference voltage at the duty cycle of the PWM signal. The pulse signal is then filtered by an internal low-pass filter. SGM37604S regulation voltage is independent of the PWM logic voltage level which often has large variations.

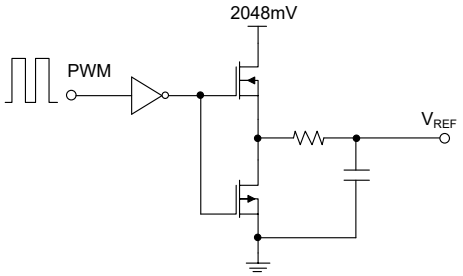


Figure 8. Programmable V_{REF} Using PWM Signal

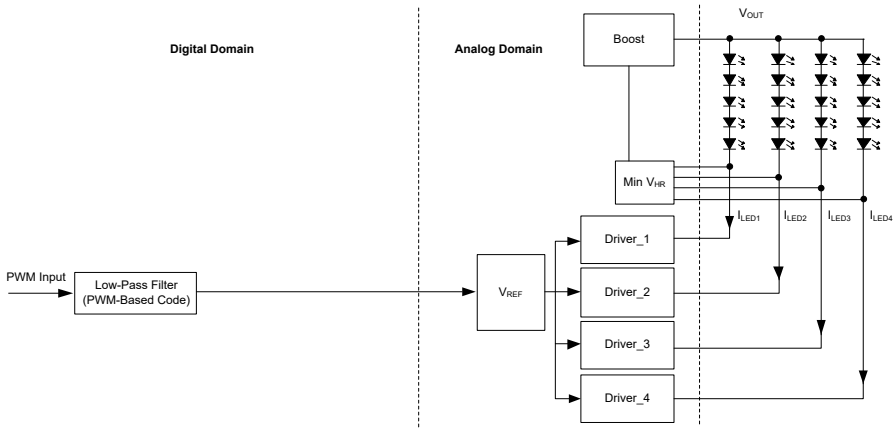


Figure 9. Brightness Control 01 (PWM Only)

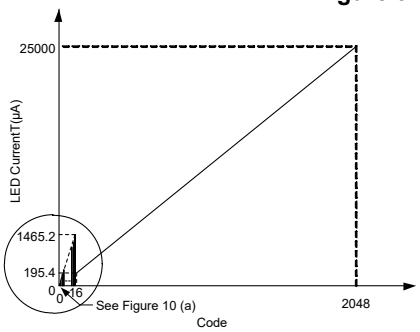


Figure 10. LED Current vs. Brightness Code (Mode 01)

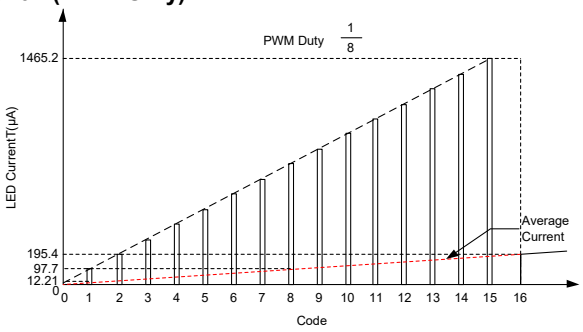


Figure 10 (a).

DETAILED DESCRIPTION (continued)

I²C + PWM (Brightness Mode 10 or 11)

In brightness control mode 10 or 11 both the I²C code and the PWM duty cycle control the LED current. The brightness code is calculated by PWM duty cycle and the I²C brightness code, and follows the relationship (see Figure 11):

When the I²C code is an odd integer,

BRT code = (I²C code - 1) × 0.5 × PWM duty cycle (6)

When the I²C code is an even integer,

BRT code = I²C code × 0.5 × PWM duty cycle (7)

where

BRT code = the brightness code

I²C codes are valid from 0 to 4095. The codes should be integers.

The average LED current increases proportionally to the brightness code and is calculated by Equation 8.

$$I_{LED\_AVG} = 12.21\mu A \times code \quad (8)$$

This is valid from codes 1 to 2047 and the codes could be integers or decimals. Code 1 programs the LED current to 12.21μA with 25mA maximum LED current. Code 0 programs 0 current (see Figure 12). When the brightness code < 16, the LED current is in current-to-PWM control. The duty cycle of the PWM is 1/8, and the amplitude of current pulse is 8 times of its corresponding average current. Figure 12 (a) shows the zoomed graph from codes 0 to 16 in Figure 12.

When bit[4] is set to 1 in REG0x11, ramp function is enabled. When bits[7:4] in REG0x19 are not all 0 (codes from 256 to 4095), regardless of PWM duty cycle, the ramp rate is 128μs/step. When bits[7:4] in REG0x19 are all 0 (codes from 1 to 255), regardless of PWM duty cycle, the ramp rate is 1024μs/step. For example, if PWM duty cycle is set to 10% and the code is set from 2000 to 4001, I_{LED_AVG} will change from 1.221mA to 2.442mA, the corresponding ramp rate = 128μs/step, so the ramp time for I_{LED_AVG} = [(4001 - 1) × 0.5 - 2000 × 0.5] × 128μs = 128ms.

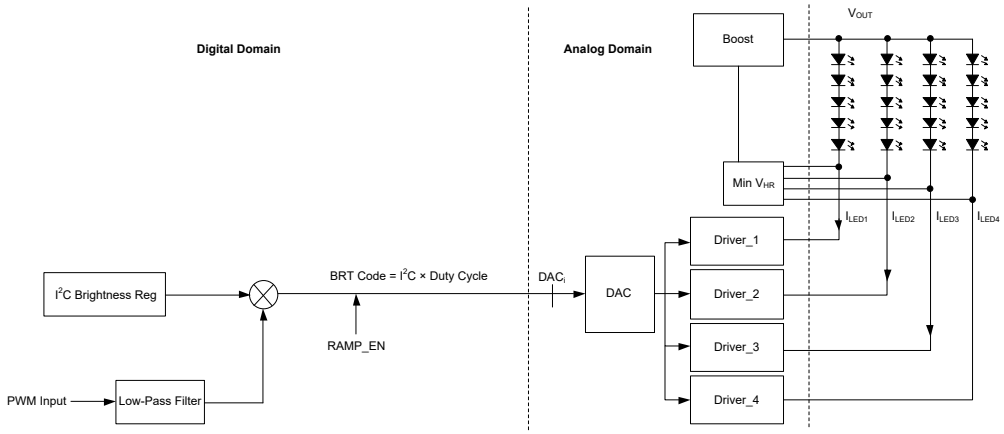


Figure 11. Brightness Control 10 or 11 (I²C + PWM)

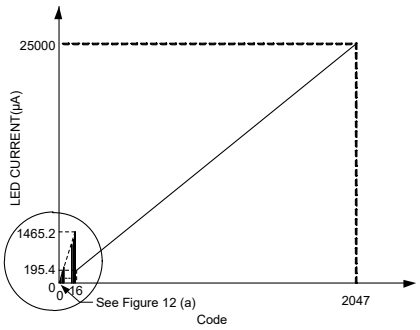


Figure 12. LED Current vs. Brightness Code (Mode 10 or Mode 11)

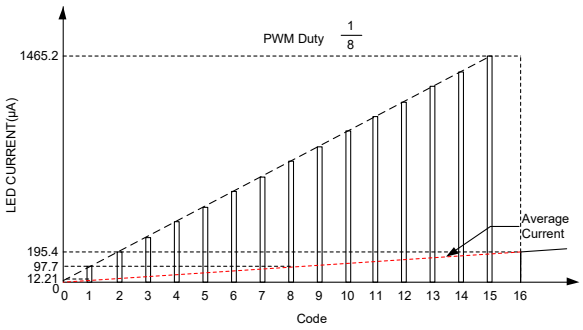


Figure 12 (a).

DETAILED DESCRIPTION (continued)

Hybrid PWM & I²C Dimming Control

Hybrid PWM & I²C dimming control combines PWM dimming and LED current-dimming control methods. With this dimming control, better optical efficiency is possible from the LEDs compared to pure PWM control while still achieving smooth and accurate control and low brightness levels. The switch point from current-to-PWM control is set to get the optimal compromise between good matching of the LEDs brightness/white point at low brightness and good optical efficiency. For I²C mode, the LED current enters current-to-PWM control when bits[7:4] in REG0x19 are all 0. For other modes, the LED current enters current-to-PWM control when the brightness code < 16 (See Brightness Control Modes).

Phase Shift PWM Scheme

The phase shift PWM (PSPWM) scheme allows overlapping time when each LED current sink is active. When the LED current sinks are not activated simultaneously, the peak load current from the Boost output is greatly decreased. This reduces the ripple seen on the Boost output and allows smaller output capacitors to be used. Reduced ripple also reduces the output ceramic capacitor audible ringing. The PSPWM scheme also increases the load frequency seen on the Boost output by up to three times, thus transferring the possible audible noise to the frequencies outside the audible range.

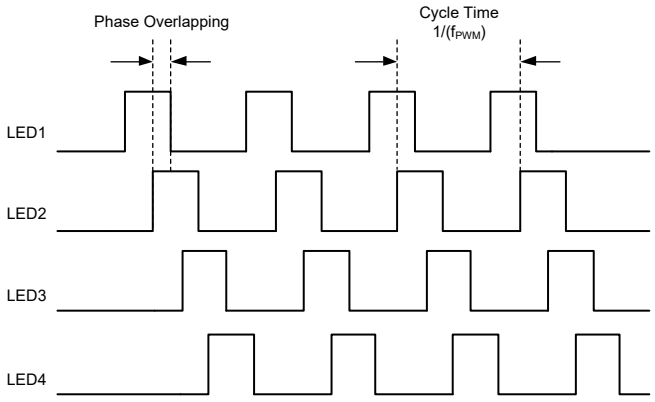


Figure 13. Phase Shift PWM Dimming Scheme Diagram

DETAILED DESCRIPTION (continued)

Fault Protection/Detection

Over-Voltage Protection (OVP)

The OVP function automatically turns off the Boost converter when the output voltage exceeds 29.5V (TYP), thereby protecting the device OUT and SW pins from high voltage damage. The OVP function is usually triggered in two different over-voltage conditions.

Case 1 OVP Fault Only (OVP threshold was triggered and no LED open circuit occurred)

As the number of LEDs per string increases approximately to maximum number of LEDs per string, the V_{OUT} may approach the OVP threshold in steady state. When the SGM37604S encounters a fast transient change of V_{IN} or LED current, V_{OUT} may suddenly increase to trigger the OVP threshold. At this point the OVP is triggered and the Boost converter stops working until the output voltage drops to the lower threshold voltage of the OVP. To avoid false triggering, the duration when V_{OUT} is higher than the OVP threshold must be longer than 1ms. In this case, the OVP fault flag (REG0x1F[0]) is set to 1.

Case 2 LED String Open Fault (OVP threshold triggers and an LED open circuit occurs)

When the LED open fault occurs, the Boost converter detects that V_{HR} is lower than 40mV, and the Boost control loop will operate with maximum on-time that results in V_{OUT} to increase, which ultimately results in boost to trigger OVP. When LED open occurs, the Boost converter is disabled and the output voltage is reduced. At this time, the OVP fault flag (REG0x1F[0]) and the LED open fault flag (REG0x1F[4]) are both set to 1.

LED Short Fault

The SGM37604S implements LED short fault protection. The device monitors the current sink input voltage, as the voltage exceeds 16V, the device will trigger LED short fault protection. At this time, both the Boost converter and the current sinks will stop working and the device will enter the standby state. In addition, if the current sink input voltage does not exceed 16V when the LED short occurs, the device will not trigger the LED short fault protection.

Over-Current Protection (OCP)

The SGM37604S has OCP threshold (2.35A, TYP). The device constantly monitors the current flowing through the low-side NFET. When the current exceeds the OCP threshold, the NFET is turned off immediately for the remaining period of the switching period.

When the OCP is continuously triggered, the device sets the OCP fault flag bit (REG0x1F[1]) to 1. The SGM37604S has a built-in counter that can monitor OCP events over a period of 128μs. If 32 consecutive OCP triggering events occur for 128μs periods, the REG0x1F[1] bit is set to 1, so there is a 4ms blank time more or less.

Over-Temperature Protection (OTP)

When the temperature of the device exceeds +155℃, over-temperature protection (OTP) is triggered, the device stops working, and the OTP Fault flag (REG0x1F[2]) is set to 1. When the temperature of the device drops to +130℃, the device will restart.

LEDx Pin Unused

As shown in Figure 14, user can easily disable the unused channel by connecting its LEDx pin to GND pin or leaving it floating.

DETAILED DESCRIPTION (continued)

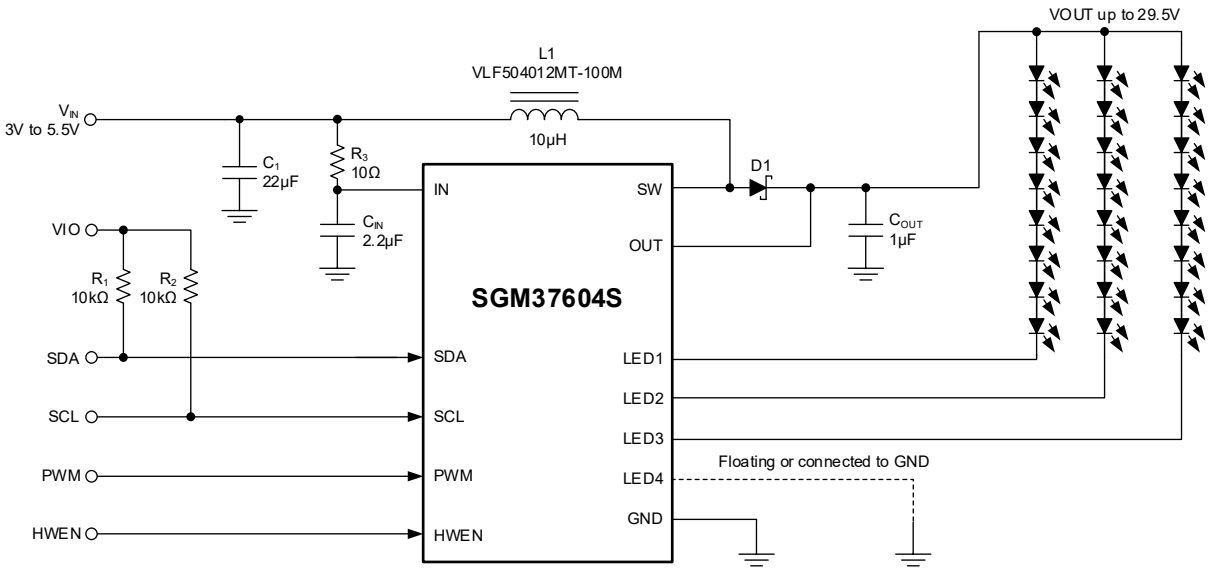


Figure 14. Typical Application for Less than Four Parallel LED Strings

I²C Interface

Start and Stop Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 15. All transactions begin by the master who applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is when SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP, the bus is considered busy.

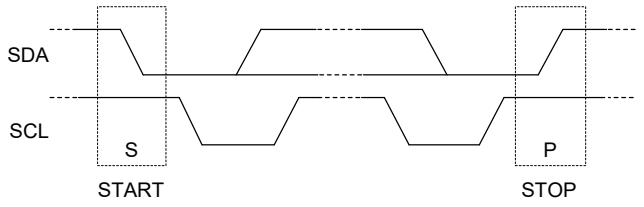


Figure 15. I²C Start and Stop Conditions

I²C Address

The SGM37604S operates as a slave device with address 0x36 (36H). It has seven 8-bit registers. The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/W). R/W bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accessed in the next byte(s). The third byte contains the data for the selected register.

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. If the slave is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the master in a wait state. When the slave is ready for another byte of data, it releases the clock line and data transfer can continue with clocks generated by master.

Register Programming

For glitch free operation, the bits[6:5] in REG0x11 (Brightness Mode) and bit[4] in REG0x11 (Ramp Enable) should only be programmed while the LED Enable bits are 0 (REG0x10[4:1] = 0000) and Device Enable bit is 1 (REG0x10[0] = 1).

APPLICATION INFORMATION

The SGM37604S is a high-precision and small-size LED backlight driver solution for consumer applications such as tablet or laptop computers. The device implements the Boost converter plus current sink architecture, which can effectively support multi-string LED backlight panels while supporting high precision dimming.

To maximize the performance, appropriate external components selection is required. Table 2 provides recommended part numbers for inductors, Schottky diodes, and output capacitors in different LED configurations.

Table 2. Typical Application Component List

Configuration	L1	D1	C_{OUT}
4P7S, 4P8S	VLF504012MT-100M VLF504012MT-150M	NSR0530P2T5G	C2012X7R1H105K085AC
4P6S	VLF504012MT-220M	NSR0530P2T5G	C2012X7R1H105K085AC
4P5S	VLF403210MT-100M	NSR0530P2T5G	C2012X7R1H105K085AC
4P4S	VLF302510MT-100M	NSR0530P2T5G	C2012X7R1H105K085AC

Component Selection

Inductor

The SGM37604S requires a typical 10μH inductance. The selection of inductors is mainly concerned with saturation current value and inductance value. The saturation current value of the inductor should be higher than the inductive current peak (I_{PEAK}) under the worst conditions with a 30% margin. The worst case peak inductor current occurs at the minimum input voltage, minimum switching frequency, maximum output voltage and maximum load current. When the application has high transmission efficiency requirements, the peak current should be reduced as much as possible to decrease loss. I_{PEAK} can be estimated using Equation 9:

$$I_{PEAK} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} + \frac{V_{IN}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{IN} \times \eta}{V_{OUT}}) \quad (9)$$

In addition, in order to ensure the normal operation of OCP function, the inductance peak current I_{PEAK} should be lower than the OCP threshold.

Output Capacitor

To ensure the stability over the entire operating range, the recommended effective output ceramic capacitance must be higher than 0.4μF. Considering the potential tolerance, temperature, and DC derating of the ceramic capacitor, it is recommended to use a 1μF or 2.2μF ceramic capacitor as the output ceramic capacitor.

Table 3 shows the recommended output capacitor part numbers.

Equation 10 determines the effective output voltage range of the selected capacitor:

$$\text{DC Voltage Dereating} \geq \frac{0.38\mu F}{(1 - TOL) \times (1 - TEMP\_CO)} \quad (10)$$

For example, when the tolerance is 10% and the temperature coefficient is 15%, DC voltage derating ≥ 0.5μF. Typically, the capacitors in Table 3 are sufficient to meet the needs of most LED backlight driver applications. When larger capacity capacitors or greater system stability are required, two ceramic capacitors can be connected in parallel.

Input Capacitor

The recommended input capacitor is 2.2μF ceramic capacitor, which should be placed as close as possible to the IN pin of the device to be used as a filter for the input power supply.

Table 3. Recommended Output Capacitors

Part Number	Manufacturer	Case Size	Voltage Rating (V)	Nominal Capacitance (μF)	Tolerance (%)	Temperature Coefficient (%)	Recommended Max Output Voltage (For Single Capacitor)
C2012X5R1H105K085AB	TDK	0805	50	1	±10	±15	22
C2012X5R1H225K085AB	TDK	0805	50	2.2	±10	±15	24
C1608X5R1V225K080AC	TDK	0603	35	2.2	±10	±15	12
C1608X5R1H105K080AB	TDK	0603	50	1	±10	±15	15

LAYOUT

Layout Guidelines

Due to the presence of parasitic inductors and capacitors of the circuit board, SW pin of the Boost converter will exhibit spike voltage, which may cause damage to the device. In addition, parasitic parameters in the layout of the circuit board can also cause a surge in the circuit flowing through the Schottky diode and the output capacitor, which poses a threat to the power device. Figure 16 shows the analysis of the PCB parasitics that generate the undesired voltage spikes. The voltage spike of SW and the high pulse current through the Schottky diode can be effectively suppressed by reasonable circuit board layout design.

The good layout practice of SGM37604S can follow the conventional Boost converter. The current loop from the Schottky diode to the output capacitor return to the IC's ground pin should be as small as possible. In addition, in order to minimize the radiation of the SW node, the area of the SW node should be reduced as much as possible, while keeping the SW node away from other traces. The input capacitor should be placed as close as possible to the IN pin of the device to provide a stable device power supply.

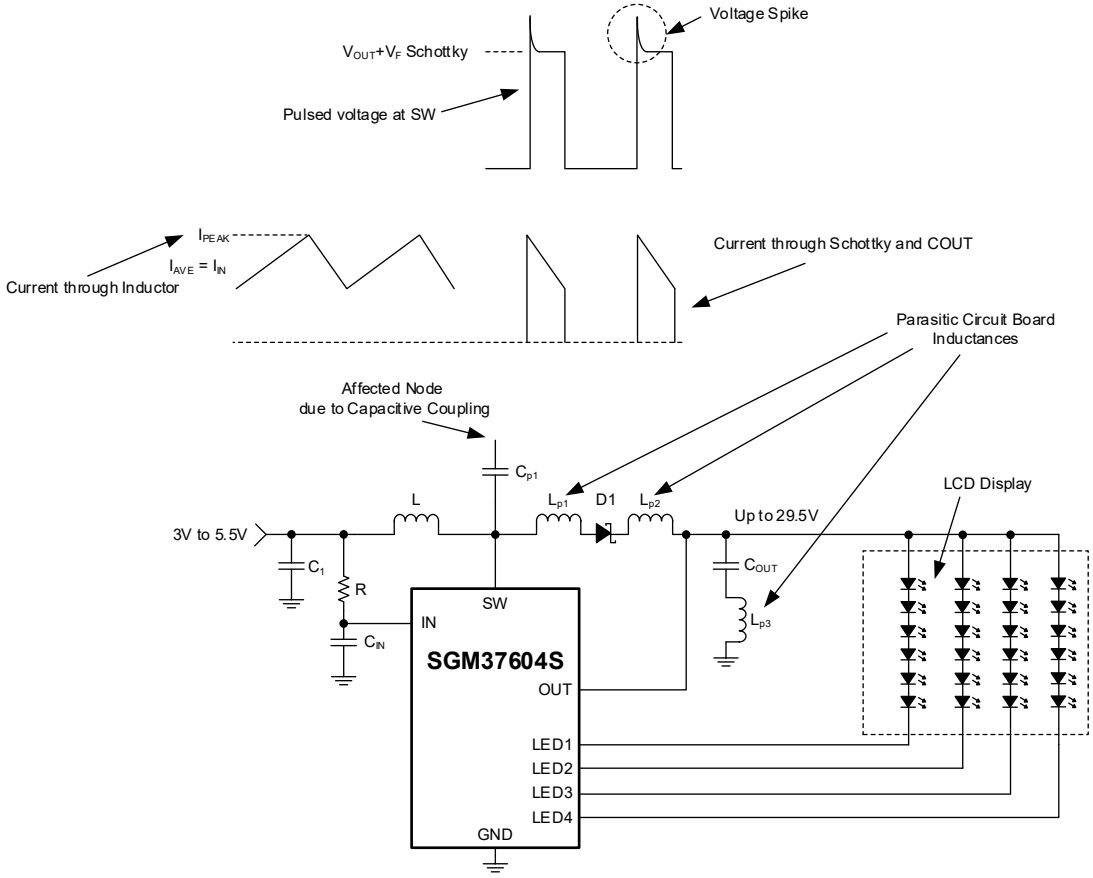


Figure 16. SW Pin Voltage (High dV/dt) and Current through Schottky Diode and C_{OUT} (High di/dt)

LAYOUT (continued)

Boost Output Capacitor Placement

In the Boost converter, whenever the NMOS is turned off and the Schottky diode is forward biased, both the output capacitor and the Schottky diode detect a high current pulse from 0 to I_{PEAK}. The current path of the output loop starts from the SW node, then passes through the Schottky diode and output capacitor, and finally returns to the GND pin of the SGM37604S. The circuit board layout parasitic parameter will cause the SW voltage spike and the high current pulsation of the Schottky diode. In order to reduce this effect, the area surrounding the SW pin, Schottky diode and output capacitor should be minimized as much as possible, so as to reduce the influence caused by parasitic parameters. The output capacitor should be placed on the same layer as the SGM37604S to avoid interference to the output current loop caused by parasitic inductance caused by the through hole.

Schottky Diode Placement

Similar to output capacitors, Schottky diodes are in the current discharge loop. Therefore, parasitic parameters in the board layout can cause SW voltage spike and Schottky diode high current pulsation. The area surrounding the SW pin, Schottky diode and output capacitance of SGM37604S should be minimized as much as possible to reduce the influence caused by parasitic parameters. Besides, Schottky diodes should be arranged in the same layer as the SGM37604S.

Inductor Placement

The inductor is an important part of the Boost converter. It is connected to the SGM37604S at the SW node. The SW node has a large dV/dt, and the SW node voltage will jump between 0 and V_{SW_PEAK} when the NMOS is turned on and off. When the SW voltage is coupled to nearby nodes through parasitic capacitors on the circuit board, it may cause interference to other key traces. For this purpose, the area of the SW node needs to be reduced as much as possible. That is to say, the inductor and the anode of the Schottky diode are as close to the SW node as possible, and the SW node is away from other critical traces. In addition, the inductance flows through a large input current, so any parasitic resistance along the path will cause the SGM37604S input voltage dropping, which reduces the efficiency and the input operating voltage range. The input capacitor should be as close to the inductor as possible to reduce the parasitic resistance on the input power line.

Boost Input Capacitor Placement

The input capacitor of SGM37604S is used to filter the input power supply. In order to ensure the stability of the power supply of SGM37604S, the input capacitor should be as close as possible to the IN pin of the device to avoid voltage spikes in the IN pin caused by parasitic parameters, which may affect the normal operation of SGM37604S.

PCB Layout

Figure 17 shows an example of SGM37604S PCB layout.

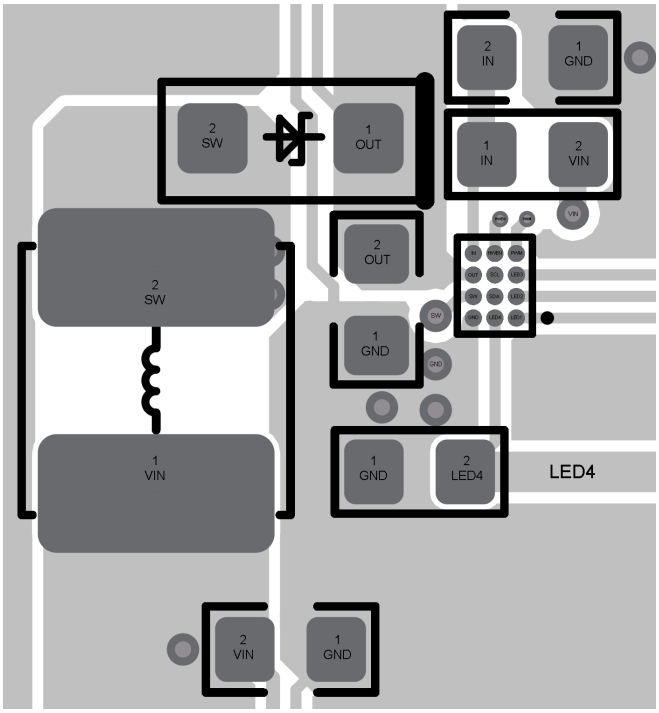


Figure 17. Layout Example

REVISION HISTORY

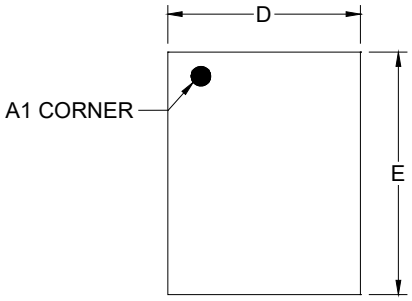
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

AUGUST 2024 – REV.A to REV.A.1	Page
Updated Typical Performance Characteristics section	7

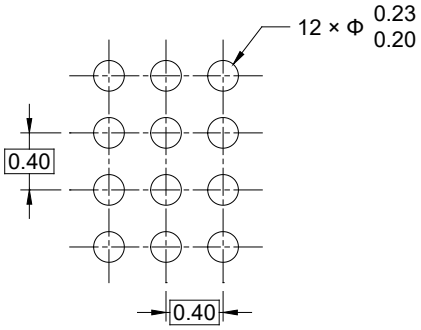
Changes from Original (JUNE 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

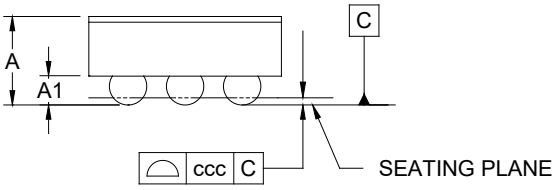
WLCSP-1.35×1.7-12B



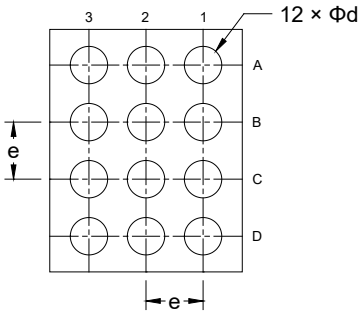
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



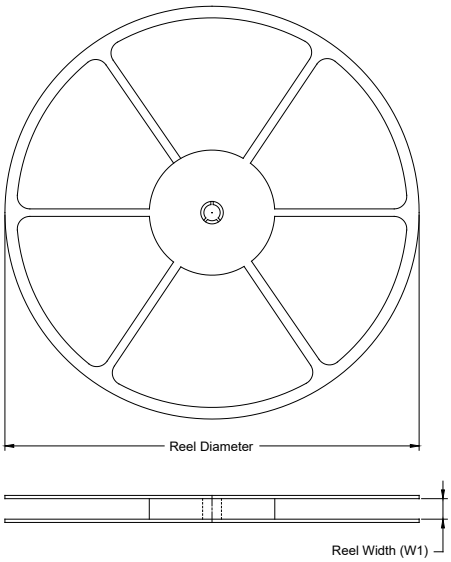
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.658
A1	0.182	-	0.222
D	1.320	-	1.380
E	1.670	-	1.730
d	0.232	-	0.292
e	0.400 BSC		
ccc	0.050		

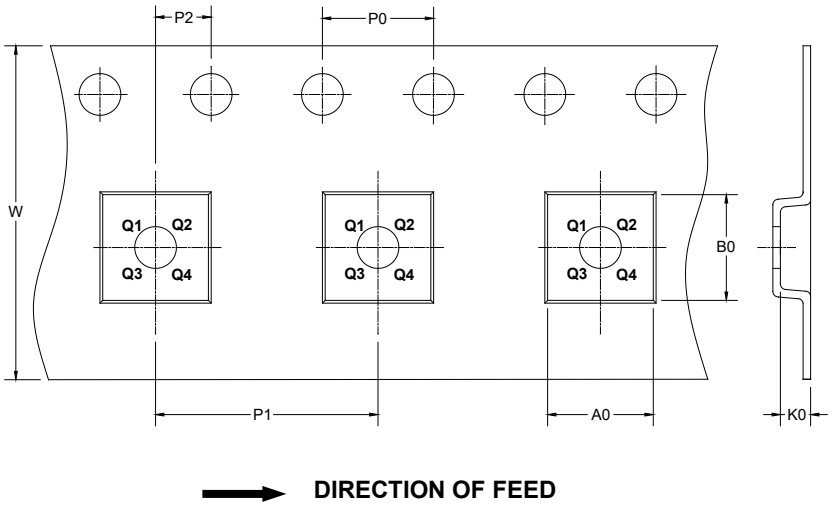
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



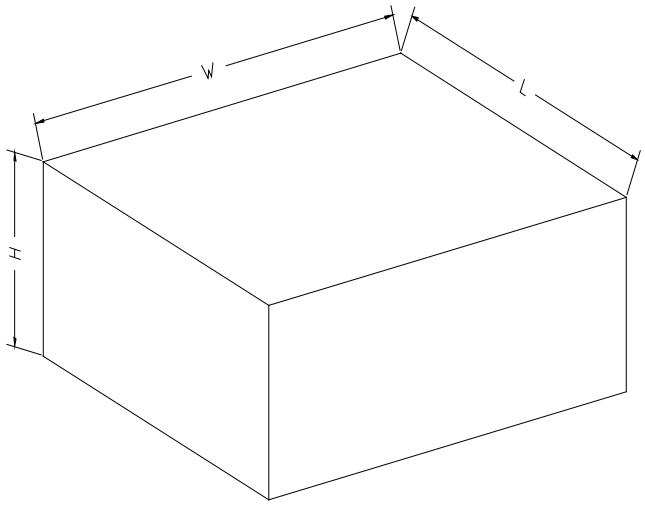
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.35×1.7-12B	7"	9.5	1.46	1.90	0.81	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002