SGM5355-16
16-Bit, I²C Interface, Voltage-Output Digital-to-Analog Converter

GENERAL DESCRIPTION

The SGM5355-16 is a low power, single channel, 16-bit, voltage-output DAC. It operates from a 2.7V to 5.5V supply and the monotonicity is guaranteed by design.

The SGM5355-16 sets the output range by using an external reference voltage. It incorporates a power-on reset circuit that ensures the DAC output powers to 0V and remains powered up at this level until a valid write takes place. The SGM5355-16 provides a power-down mode accessed via the serial interface that reduces the current consumption of the device to 450nA (TYP) at 5.5V. The SGM5355-16 consumes 0.27mW (TYP) at 2.7V in normal mode, which reduces to less than 1μW in power-down mode. The low power consumption in normal mode is very suitable for portable battery-operated equipment.

The SGM5355-16 uses a versatile 2-wire serial interface that operates at clock rates to 400kHz and is compatible with standard I²C interfaces.

The SGM5355-16 is available in Green WLCSP-0.82×1.22-6B and MSOP-8 packages. It operates over an ambient temperature range of -40℃ to +125℃.

FEATURES

- **Power Supply Range: 2.7V to 5.5V**
- **16-Bit DAC, Monotonicity Guaranteed by Design**
- **6LSB (TYP) Relative Accuracy**
- **Low Power Operation: 100μA (TYP) at 2.7V**
- **Power-On Reset to Zero-Scale**
- **10μs (TYP) Settling Time**
- **I²C Serial Interface**
- **Rail-to-Rail Buffered Voltage-Output Operation**
- **Binary Code Input**
- **Power-Down Function**
- **Available in Green WLCSP-0.82×1.22-6B and MSOP-8 Packages**

APPLICATIONS

Process Control
Data Acquisition Systems
Closed-Loop Servo-Control
PC Peripherals
Portable Instrumentation
Programmable Attenuation

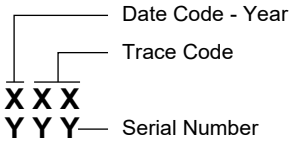
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM5355-16	WLCSP-0.82×1.22-6B	-40℃ to +125℃	SGM5355-16XG/TR	XXX SXG	Tape and Reel, 3000
	MSOP-8	-40℃ to +125℃	SGM5355-16XMS8G/TR	SGMSWH XMS8 XXXXX	Tape and Reel, 4000

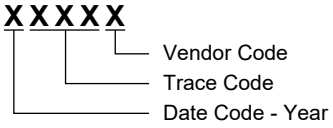
MARKING INFORMATION

NOTE: XXX = Date Code and Trace Code. XXXXX = Date Code, Trace Code and Vendor Code.

WLCSP-0.82×1.22-6B



MSOP-8



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range ..... -0.3V to 6V
Digital Input Voltage Range ..... -0.3V to V_{CC} + 0.3V
Output Voltage Range ..... -0.3V to V_{CC} + 0.3V
Package Thermal Resistance
MSOP-8, θ_{JA} ..... 168℃/W
MSOP-8, θ_{JC} ..... 65℃/W
WLCSP-0.82×1.22-6B, θ_{JA} ..... 208℃/W
WLCSP-0.82×1.22-6B, θ_{JC} ..... 165℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM ..... ±4000V
CDM ..... ±1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range (V_{CC} to GND) ..... 2.7V to 5.5V
Digital Input Voltage Range (SDA, SCL, ADDR)
..... 0V to V_{CC}
Reference Input Voltage Range, V_{REF} ..... 0V to V_{CC}
Output Amplifier Feedback Input, V_{FB} ..... V_{OUT}
Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

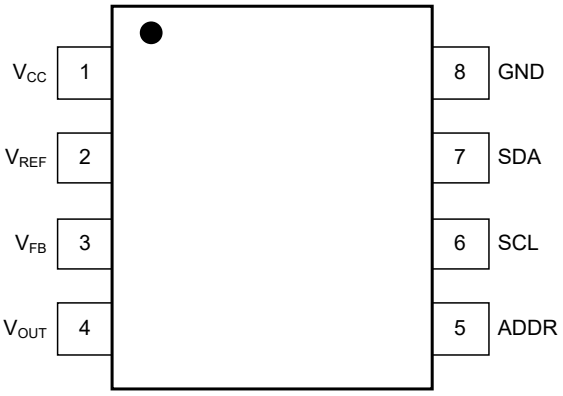
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

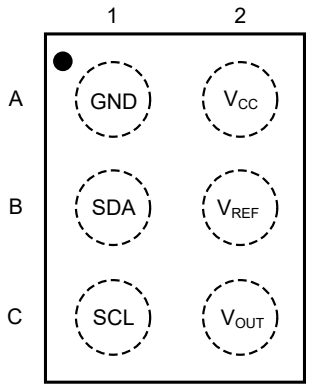
PIN CONFIGURATIONS

(TOP VIEW)



MSOP-8

(TOP VIEW)



WLCSP-0.82×1.22-6B

PIN DESCRIPTION

PIN		NAME	TYPE (1)	FUNCTION
MSOP-8	WLCSP-0.82×1.22-6B			
1	A2	V_{CC}	P	Power Supply Pin. It can be operated from 2.7V to 5.5V.
2	B2	V_{REF}	I	Reference Voltage Input Pin.
3	–	V_{FB}	I	Output Amplifier Feedback Input Pin. Connect to V_{OUT} externally for the voltage-output operation.
4	C2	V_{OUT}	O	Analog Output Voltage from DAC. The output amplifier has rail-to-rail operation.
5	–	ADDR	I	I^2C Address Selection Pin. It can be tied to SDA, GND, V_{CC}, and SCL. See detail in Table 1.
6	C1	SCL	I	I^2C Clock Signal. Data can be transferred at rates to 400kHz Schmitt-Trigger logic input.
7	B1	SDA	I/O	I^2C Data Signal. Transmits and receives data.
8	A1	GND	G	Ground Pin.

NOTE:
1. I = Input, O = Output, I/O = Input or Output, P = Power, G = Ground.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 5.5V, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Static Performance (1)						
Resolution			16			Bits
Relative Accuracy	INL	Measured by line passing through codes 485 and 64741 at V_{REF} = 5.4V, codes 970 and 63947 at V_{REF} = 2.5V		6	14	LSB
Differential Nonlinearity	DNL	2.5V ≤ V_{REF} ≤ 5.5V, -40℃ ≤ T_A ≤ +125℃		0.5	1	LSB
Zero-Code Error		Measured by line passing through codes 485 and 64741		0.55	3.5	mV
Full-Scale Error		Measured by line passing through codes 485 and 64741		0.06	0.3	% of FSR
Gain Error		Measured by line passing through codes 485 and 64741		0.05	0.2	% of FSR
Zero-Code Error Drift				4		μV/℃
Gain Temperature Coefficient				1		ppm of FSR/℃
Power-Supply Rejection Ratio	PSRR	R_L = 2kΩ, C_L = 200pF		0.15		mV/V
Output Characteristics (2)						
Output Voltage Range			0		V_{REF}	V
Output Voltage Settling Time		R_L = 2kΩ, C_L = 50pF		10		μs
Slew Rate				1		V/μs
Capacitive Load Stability		R_L = ∞		2		nF
		R_L = 2kΩ		10		
Code Change Glitch Impulse		1LSB change around major carry		20		nV-s
Digital Feedthrough		50kΩ series resistance on digital lines		0.1		nV-s
DC Output Impedance		At mid-code input		0.3		Ω
Short-Circuit Current		V_{CC} = 5V		38		mA
		V_{CC} = 3V		36		
Power-Up Time		Coming out of power-down mode, V_{CC} = 5V		16		μs
		Coming out of power-down mode, V_{CC} = 3V		14		
AC Performance						
Signal-to-Noise Ratio	SNR	BW = 20kHz, V_{CC} = 5V, f_{OUT} = 1kHz, 1st 19 harmonics removed for SNR calculation		54		dB
Total Harmonic Distortion	THD	BW = 20kHz, V_{CC} = 5V, f_{OUT} = 1kHz, 1st 19 harmonics removed for SNR calculation		-62		dB
Spurious-Free Dynamic Range	SFDR	BW = 20kHz, V_{CC} = 5V, f_{OUT} = 1kHz, 1st 19 harmonics removed for SNR calculation		66		dB
Signal-to-Noise and Distortion	SINAD	BW = 20kHz, V_{CC} = 5V, f_{OUT} = 1kHz, 1st 19 harmonics removed for SNR calculation		53		dB
Reference Input						
Reference Input Current		V_{REF} = V_{CC} = 5V		21	26	μA
		V_{REF} = V_{CC} = 3.6V		15	22	
Reference Input Range			0		V_{CC}	V
Reference Input Impedance				235		kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.7V to 5.5V, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Inputs (2)							
Input Current					10		nA
Input Low Voltage	V_{IL}	V_{CC} = 5.5V				1	V
		V_{CC} = 2.7V				0.6	
Input High Voltage	V_{IH}	V_{CC} = 5.5V		2.1			V
		V_{CC} = 2.7V		1.5			
Pin Capacitance					2		pF
Power Requirements							
Supply Voltage	V_{CC}			2.7		5.5	V
Supply Current	I_{CC}	Normal mode, input code = 32768, no load, does not include reference current, V_{IH} = V_{CC}, V_{IL} = GND	V_{CC} = 5.5V		108	150	μA
			V_{CC} = 2.7V		100	140	
		All power-down modes, V_{IH} = V_{CC}, V_{IL} = GND	V_{CC} = 5.5V		0.45	3	
			V_{CC} = 2.7V		0.32	2	
I_{OUT}/I_{CC} Power Efficiency		I_{LOAD} = 2mA, V_{CC} = 5V			95		%
Specified Performance Temperature				-40		125	℃

NOTES:

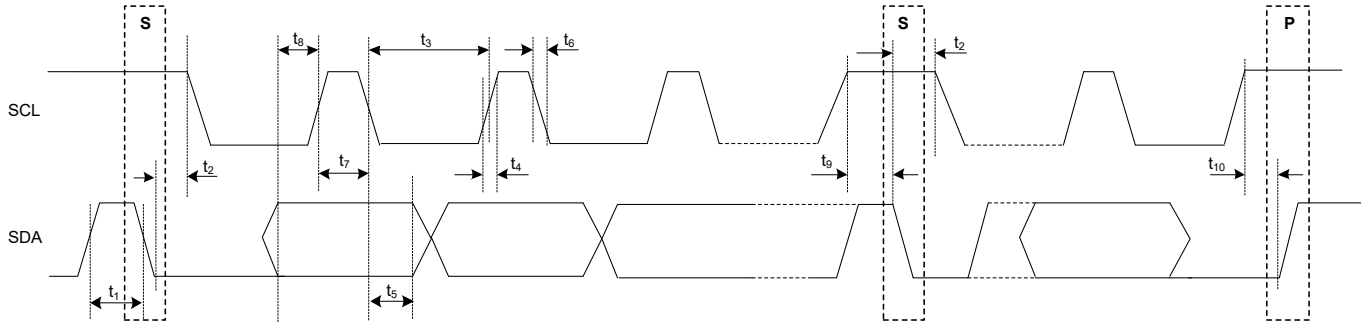
1. Linearity calculated using a reduced codes range of 485 and 64741 at V_{REF} = 5.4V, codes 970 and 63947 at V_{REF} = 2.5V; output unloaded, 100mV headroom between reference and supply.
2. Guaranteed by design. Not production tested.

TIMING CHARACTERISTICS

(V_{CC} = 2.7V to 5.5V, Full = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		UNITS
		MIN	MAX	MIN	MAX	
SCL Operating Frequency	f_{SCL}	0.01	0.1	0.01	0.4	MHz
Bus Free Time between START and STOP Condition	t_1	4700		600		ns
Hold Time after Repeated START Condition. After This Period, the First Clock is Generated.	t_2	4000		600		ns
Repeated START Condition Setup Time	t_9	4700		600		ns
Stop Condition Setup Time	t_{10}	4000		600		ns
Data Hold Time	t_5	0		0		ns
Data Setup Time	t_8	250		100		ns
SCL Clock Low Time	t_3	4700		1300		ns
SCL Clock High Time	t_7	4000		600		ns
Clock/Data Fall Time	t_6		300		300	ns
Clock/Data Rise Time	t_4		1000		300	ns

NOTE:
1. Note that t_F (MIN) for SDA output is 20ns for standard/fast mode.



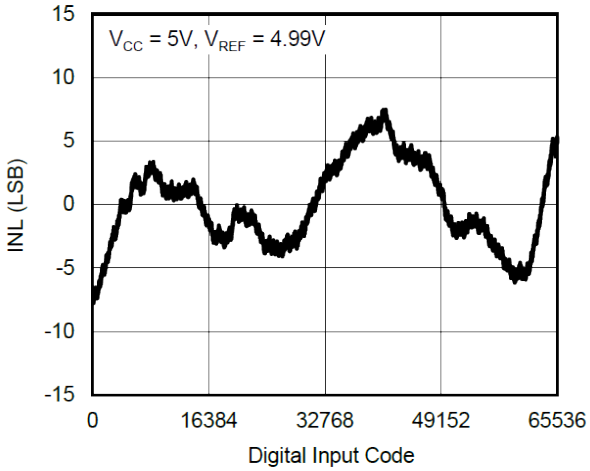
NOTE:
1. S = Start Condition, P = Stop Condition.

Figure 1. Serial Write Operation

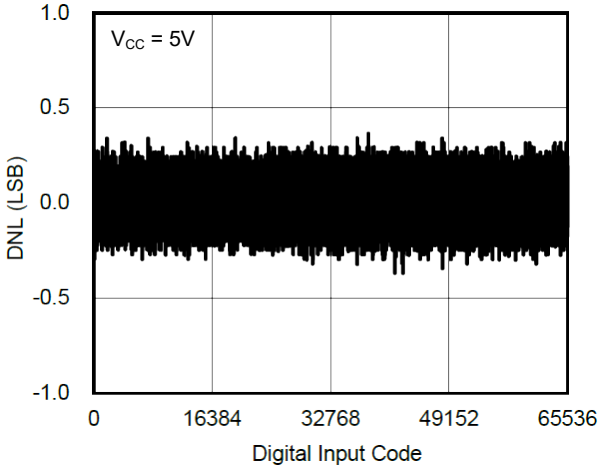
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, unless otherwise noted.

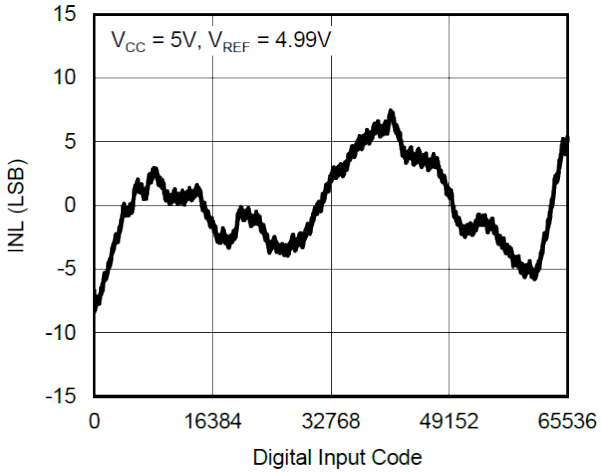
INL vs. Digital Input Code (-40℃)



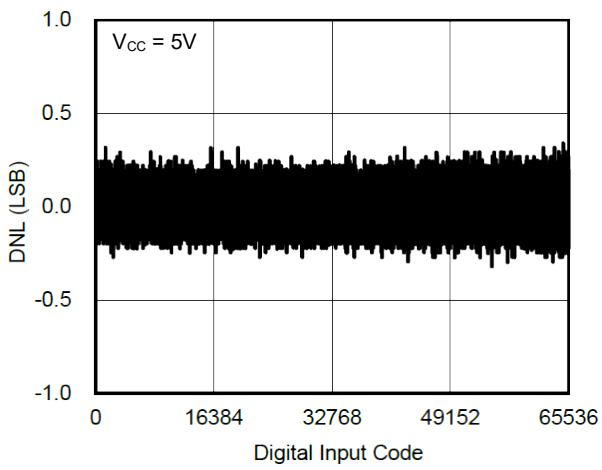
DNL vs. Digital Input Code (-40℃)



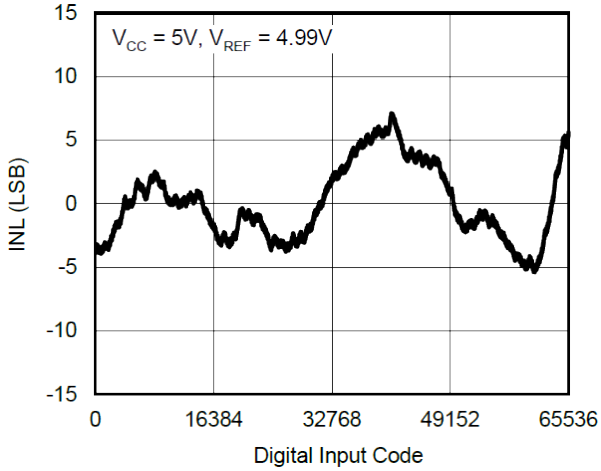
INL vs. Digital Input Code (+25℃)



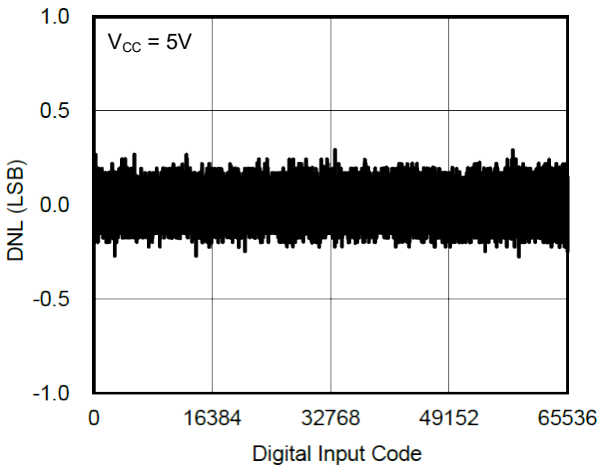
DNL vs. Digital Input Code (+25℃)



INL vs. Digital Input Code (+125℃)



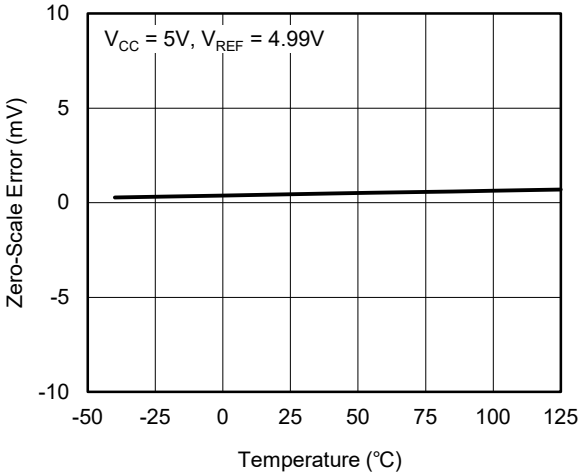
DNL vs. Digital Input Code (+125℃)



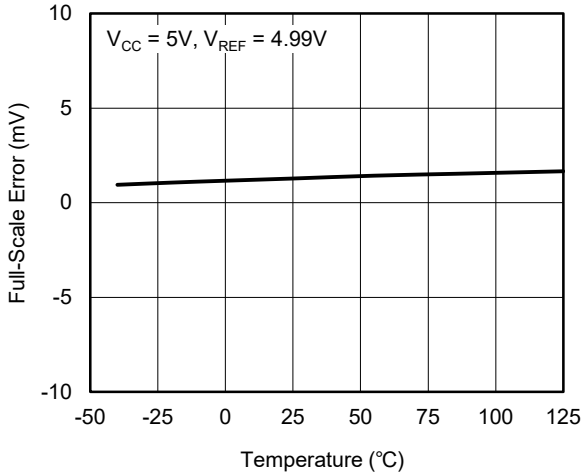
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

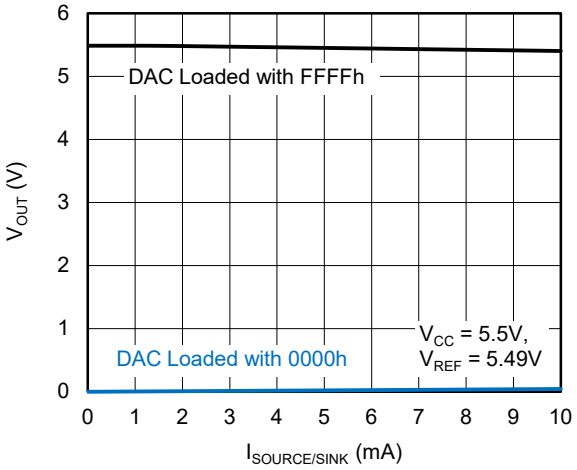
Zero-Scale Error vs. Temperature



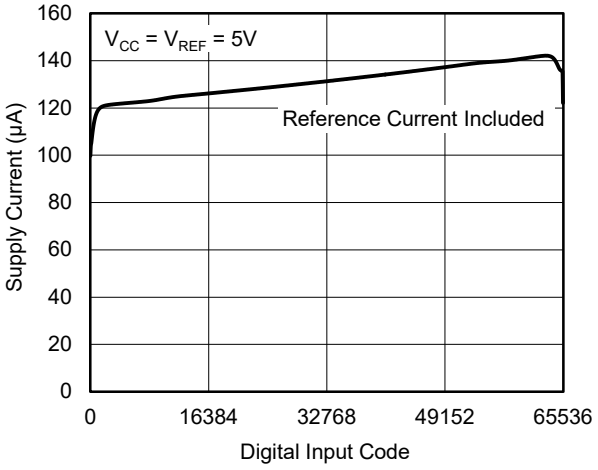
Full-Scale Error vs. Temperature



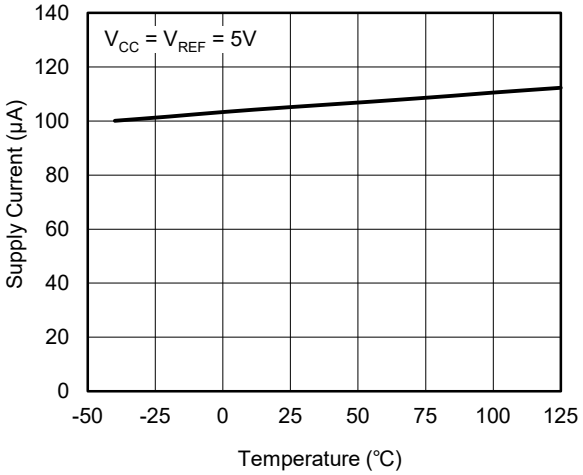
Source and Sink Current Capability



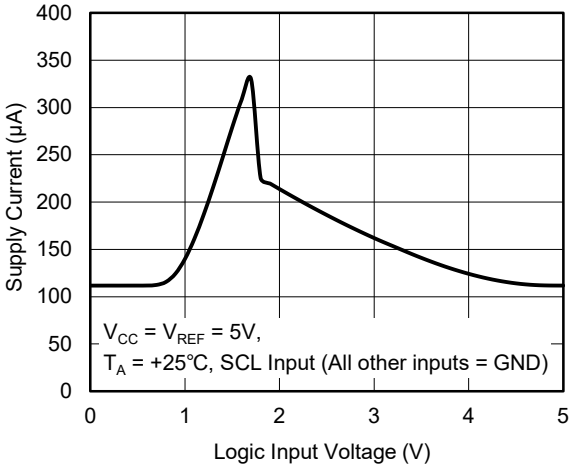
Supply Current vs. Digital Input Code



Supply Current vs. Temperature



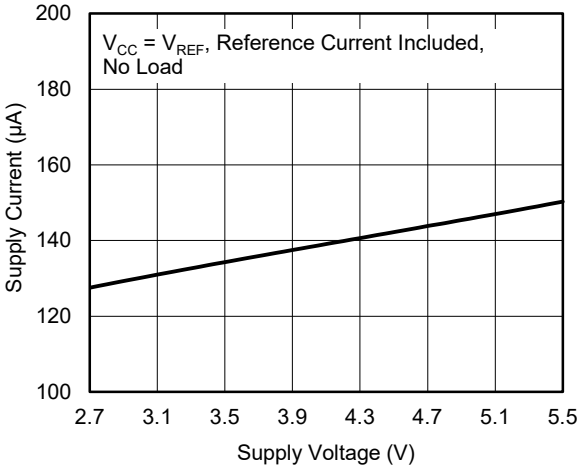
Supply Current vs. Logic Input Voltage



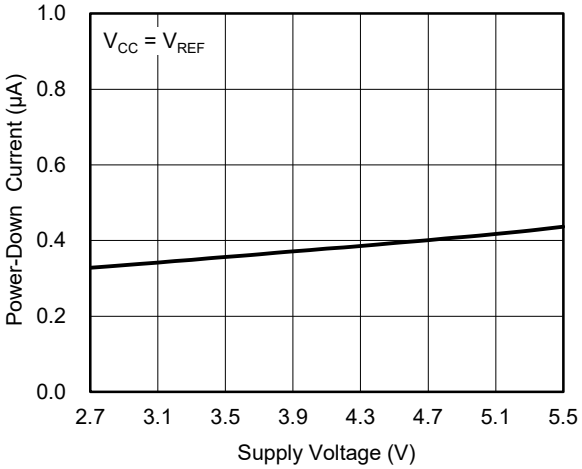
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

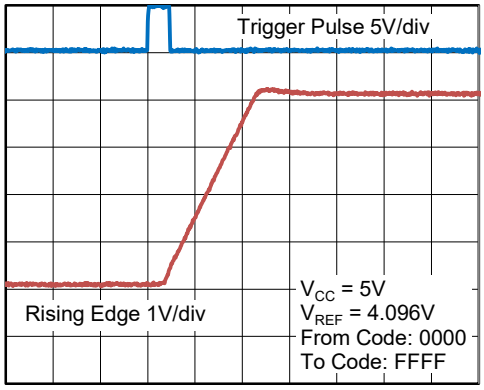
Supply Current vs. Supply Voltage



Power-Down Current vs. Supply Voltage

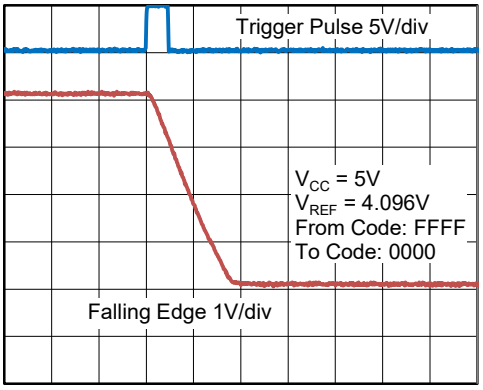


Full-Scale Settling Time, 5V Rising Edge



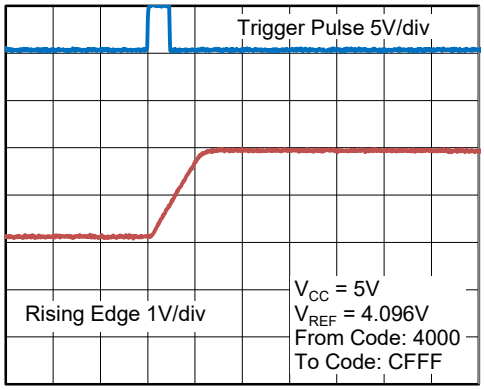
Time (2μs/div)

Full-Scale Settling Time, 5V Falling Edge



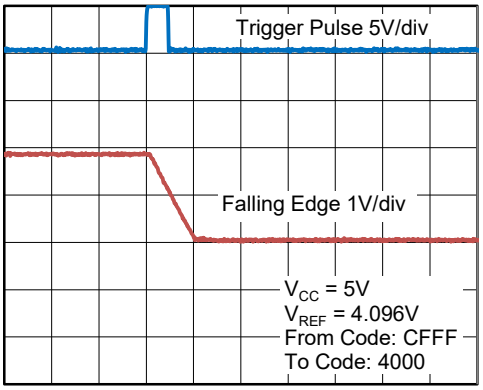
Time (2μs/div)

Half-Scale Settling Time, 5V Rising Edge



Time (2μs/div)

Half-Scale Settling Time, 5V Falling Edge

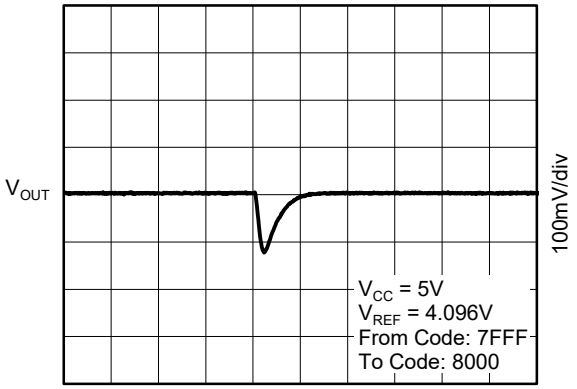


Time (2μs/div)

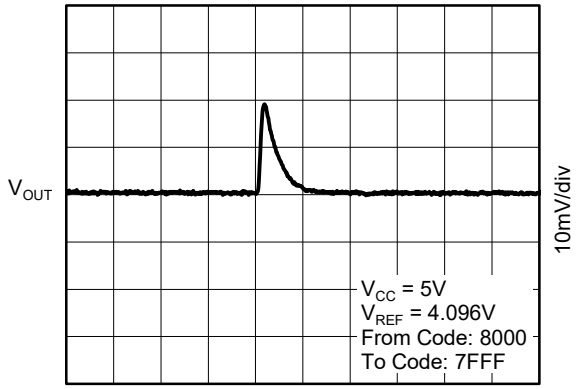
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

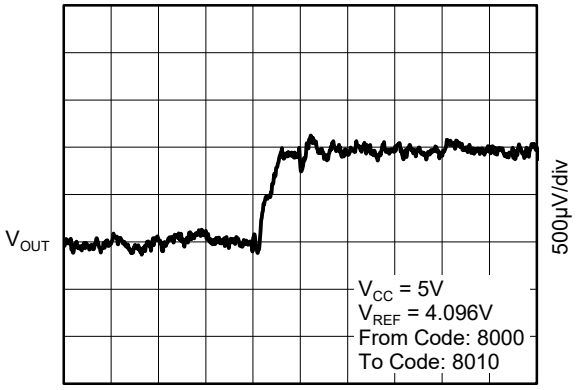
Glitch Energy: 5V, 1LSB Step, Rising Edge



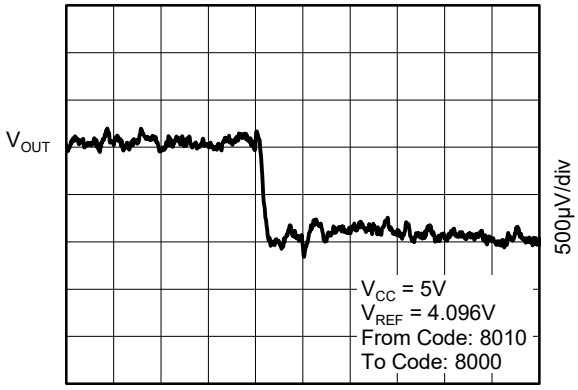
Glitch Energy: 5V, 1LSB Step, Falling Edge



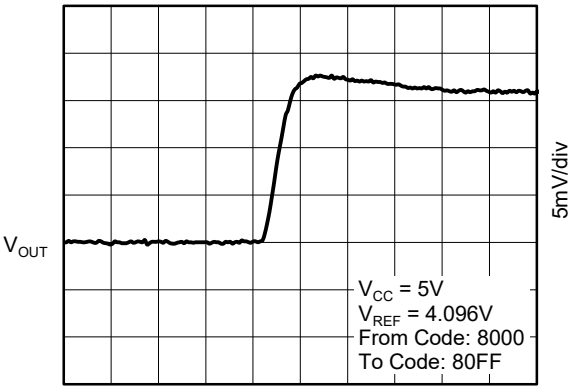
Glitch Energy: 5V, 16LSB Step, Rising Edge



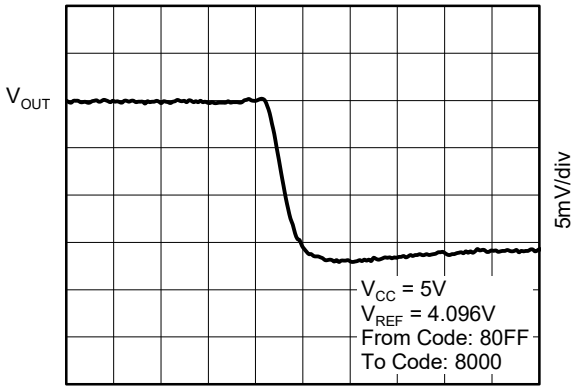
Glitch Energy: 5V, 16LSB Step, Falling Edge



Glitch Energy: 5V, 256LSB Step, Rising Edge



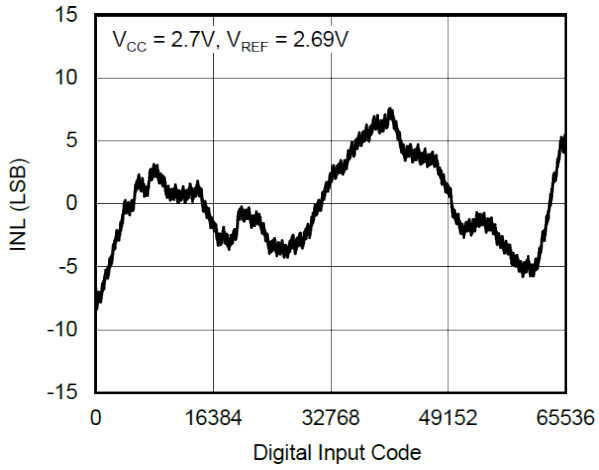
Glitch Energy: 5V, 256LSB Step, Falling Edge



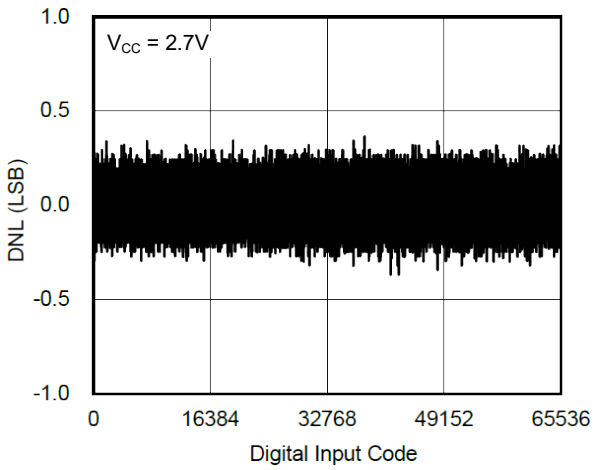
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

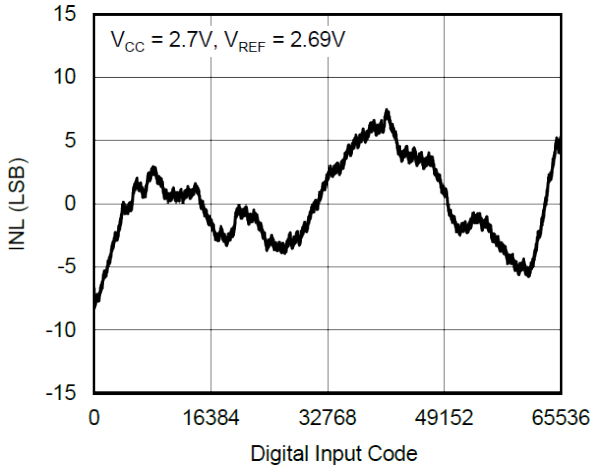
INL vs. Digital Input Code (-40℃)



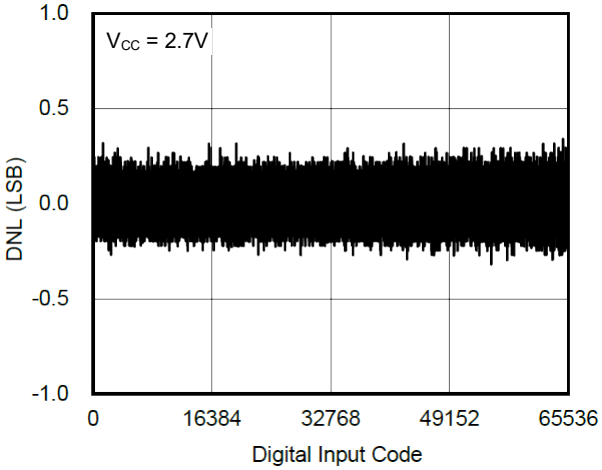
DNL vs. Digital Input Code (-40℃)



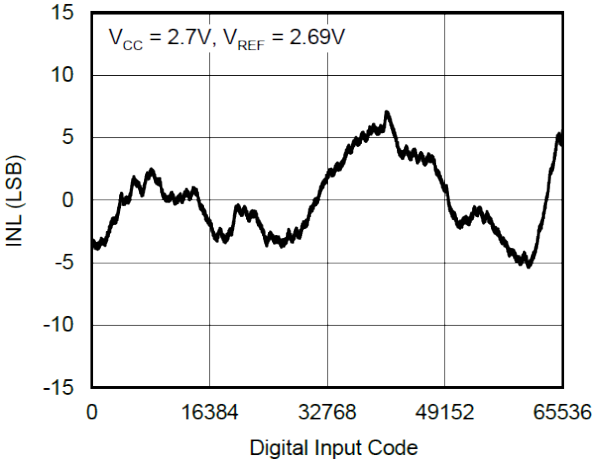
INL vs. Digital Input Code (+25℃)



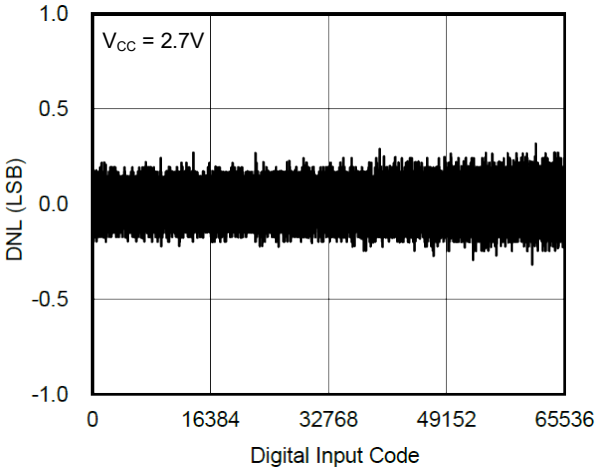
DNL vs. Digital Input Code (+25℃)



INL vs. Digital Input Code (+125℃)



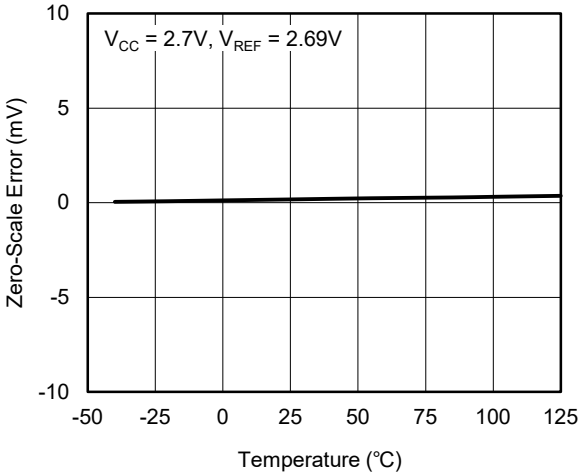
DNL vs. Digital Input Code (+125℃)



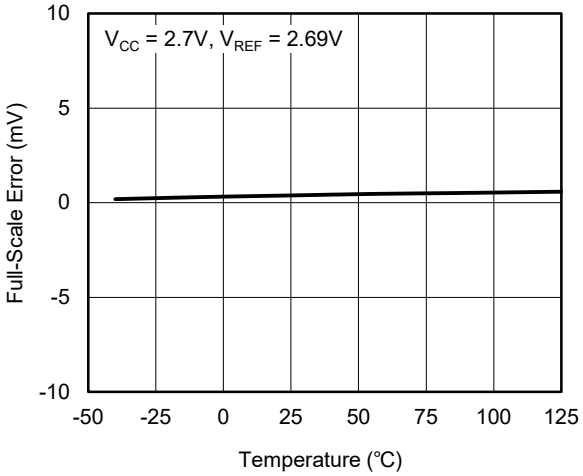
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

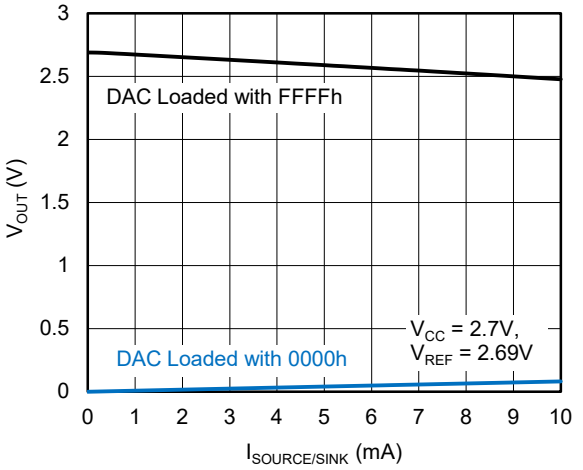
Zero-Scale Error vs. Temperature



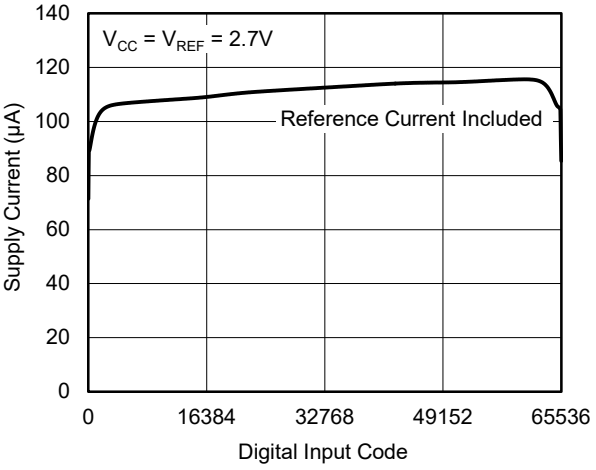
Full-Scale Error vs. Temperature



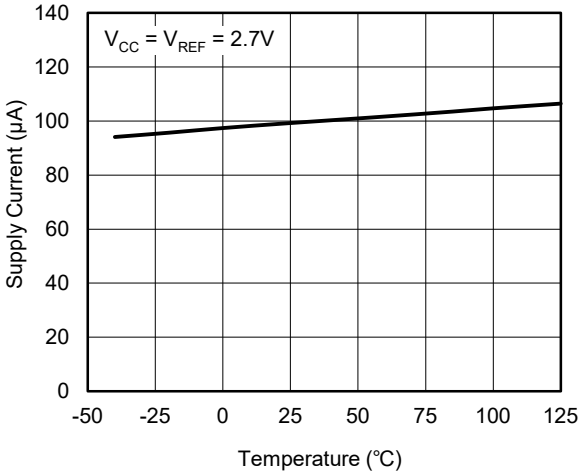
Source and Sink Current Capability



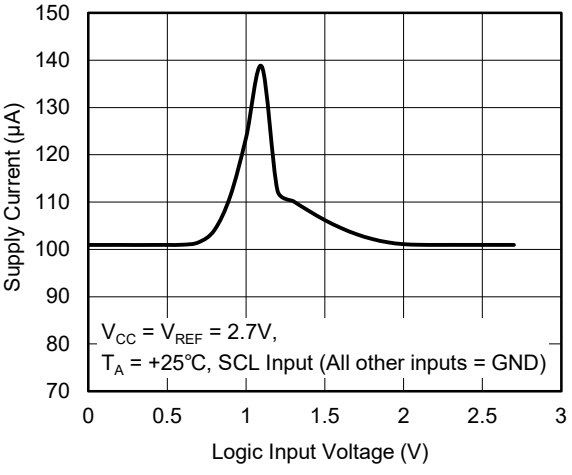
Supply Current vs. Digital Input Code



Supply Current vs. Temperature



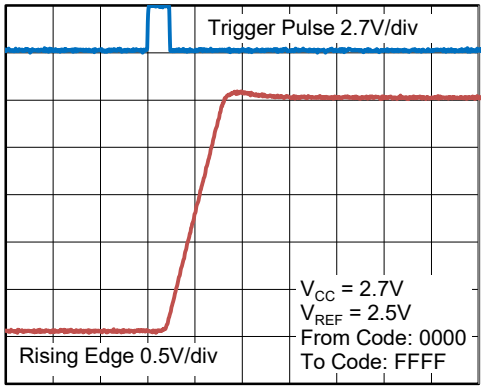
Supply Current vs. Logic Input Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

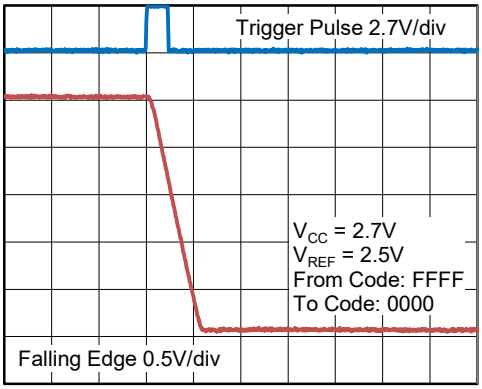
T_A = +25℃, unless otherwise noted.

Full-Scale Settling Time: 2.7V Rising Edge



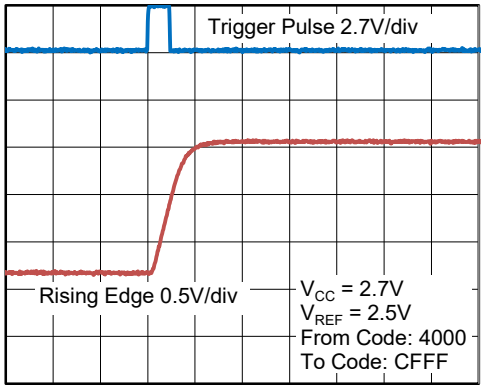
Time (2μs/div)

Full-Scale Settling Time: 2.7V Falling Edge



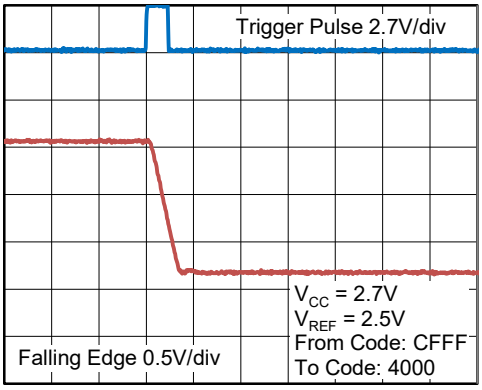
Time (2μs/div)

Half-Scale Settling Time: 2.7V Rising Edge



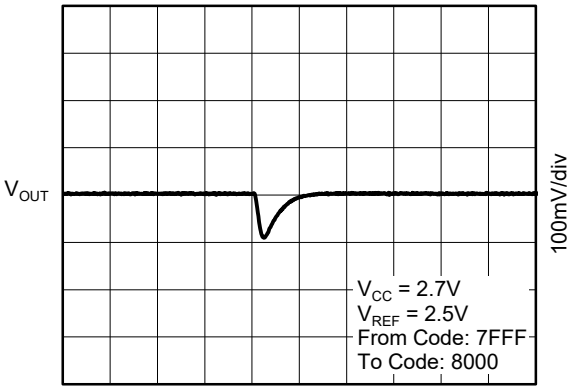
Time (2μs/div)

Half-Scale Settling Time: 2.7V Falling Edge



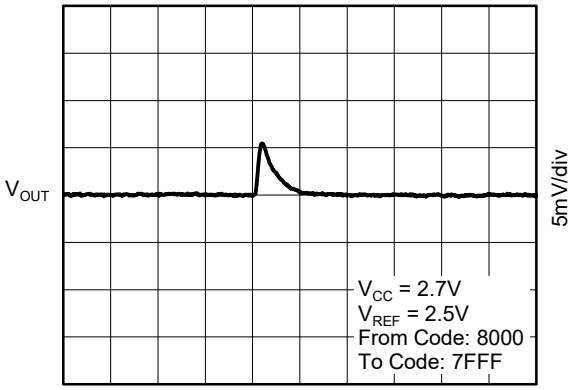
Time (2μs/div)

Glitch Energy: 2.7V, 1LSB Step, Rising Edge



Time (2μs/div)

Glitch Energy: 2.7V, 1LSB Step, Falling Edge

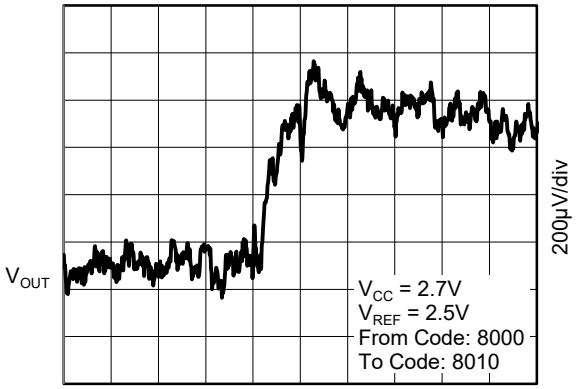


Time (2μs/div)

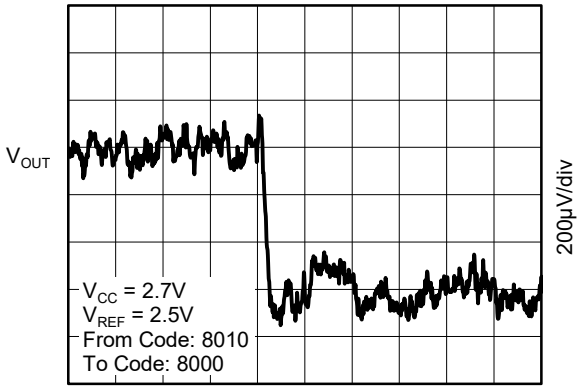
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

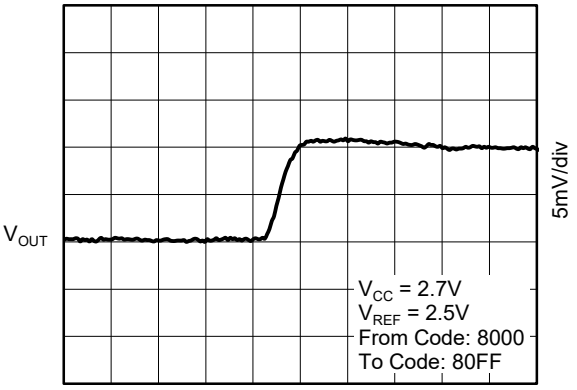
Glitch Energy: 2.7V, 16LSB Step, Rising Edge



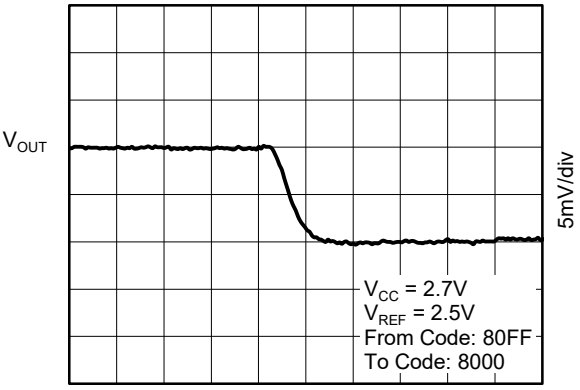
Glitch Energy: 2.7V, 16LSB Step, Falling Edge



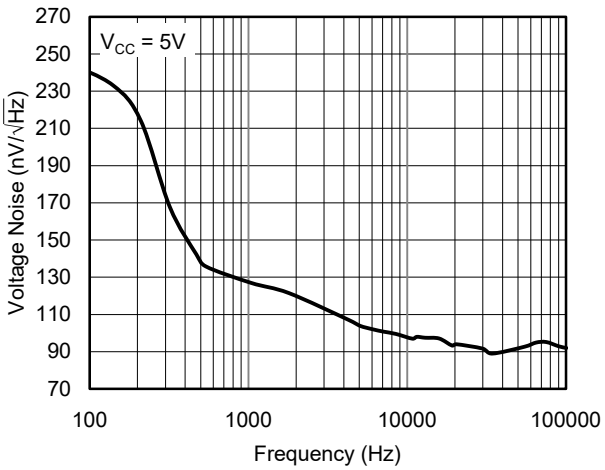
Glitch Energy: 2.7V, 256LSB Step, Rising Edge



Glitch Energy: 2.7V, 256LSB Step, Falling Edge



Output Noise Density



FUNCTIONAL BLOCK DIAGRAM

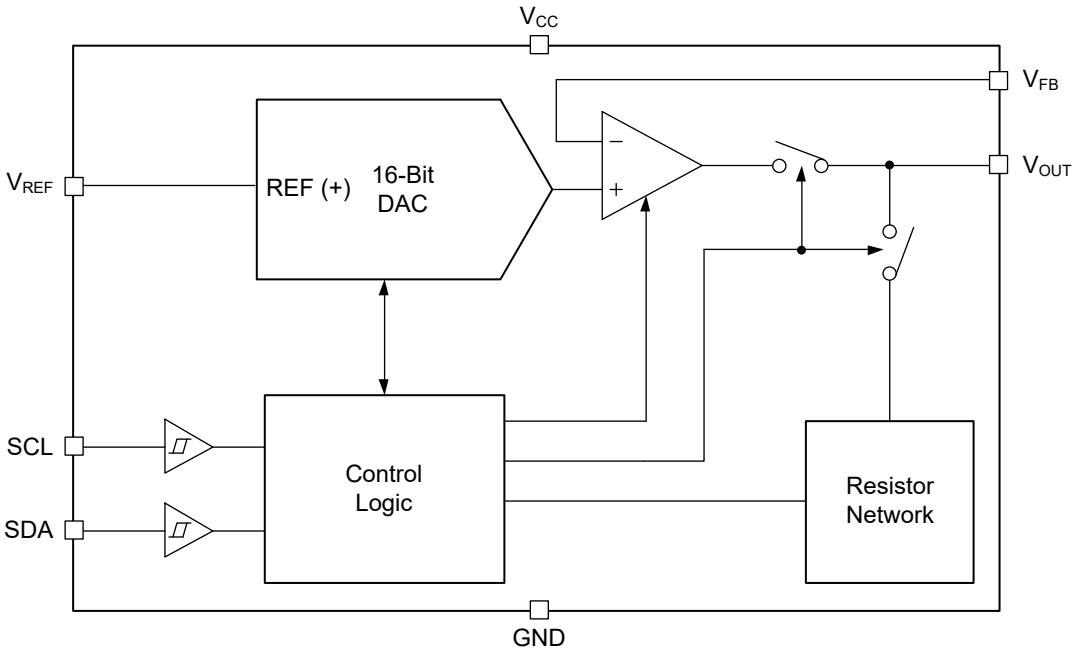


Figure 2. Block Diagram

DETAILED DESCRIPTION

DAC Section

The SGM5355-16 has an output buffer amplifier. The input code is straight binary, so the ideal output voltage can be calculated based on the following equation:

$$V_{OUT} = \frac{D_{IN}}{65536} \times V_{REF} \quad (1)$$

Where:

D_{IN} = Equal decimal code that is loaded to the DAC register, it's from 0 to 65535.

Power-On Reset

The SGM5355-16 has a power-on reset control circuit. On power-up, the DAC output voltage is 0V.

Internal Reference

The chip has no internal reference.

Programming

I²C Interface

The SGM5355-16 has a 2-wire (SCL and SDA) I²C compatible interface. See Figure 1 for a typical operation sequence.

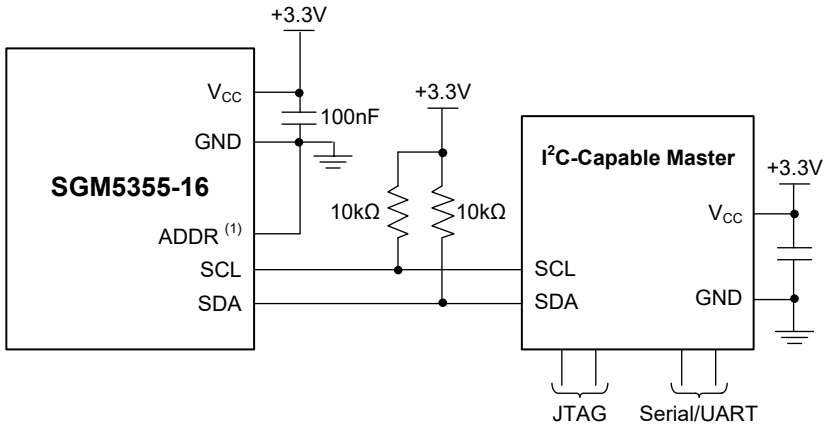
This section provides a brief example of SGM5355-16 communications. Refer to subsequent sections of this datasheet for more detailed explanations. Hardware for this design includes: one SGM5355-16 configured with an I²C address of 0001111 (WLCSP package chip's address is fixed, MSOP package chip's address can be configured by ADDR pin, see Table 1), a microcontroller with an I²C interface, discrete components such as resistors, capacitors, and serial connectors, and power supply. Figure 3 shows the basic hardware configuration.

Table 1. ADDR Pin Connection and Corresponding Slave Address

ADDR Pin	Slave Address
GND	0001101
V_{CC}	0001110
SDA	0001100
SCL	0001111

I²C Point Register Address

The SGM5355-16 has two registers that are accessible via the I²C port. The configure register allows the user to change the SGM5355-16 operating modes. Register 0x00, an 8-bit register, is the operating modes control register, the default value is 0x00, and more details are shown in Table 2 and Table 3. Register 0x01, a 16-bit register, is DAC output value control register, the default value is 0x0000, and more details are shown in Table 4.



NOTE:

1. SGM5355-16 WLCSP package doesn't have ADDR pin, and its default address is 0b0001111.

Figure 3. Basic Hardware Configuration

DETAILED DESCRIPTION (continued)

Table 2. I²C Point Register 0x00 (Default Value 0x00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	PD1	PD0
R	R	R	R	R	R	R/$\overline{W}$	R/$\overline{W}$

Table 3. Operating Modes

PD1	PD0	Operating Mode
Normal Mode		
0	0	Normal operation
Power-Down Modes		
0	1	Output typically 1kΩ to GND
1	0	Output typically 100kΩ to GND
1	1	Hi-Z

Table 4. I²C Point Register 0x01 (Default Value 0x0000)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
DB[15:8]							
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit 7	**Bit 7**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DB[7:0]							
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

I²C Writing/Reading the Registers

The SGM5355-16 works in slave mode. The master provides clock signal on the SCL pin.

In slave transmit mode, the first byte sent by the master is a 7-bit slave address followed a R/$\overline{W}$ bit. The second byte is the point address byte (which is the address of register). Refer to Table 2 and Table 4. The third and fourth bytes from the master are the bytes that to be written to the register addressed in second byte.

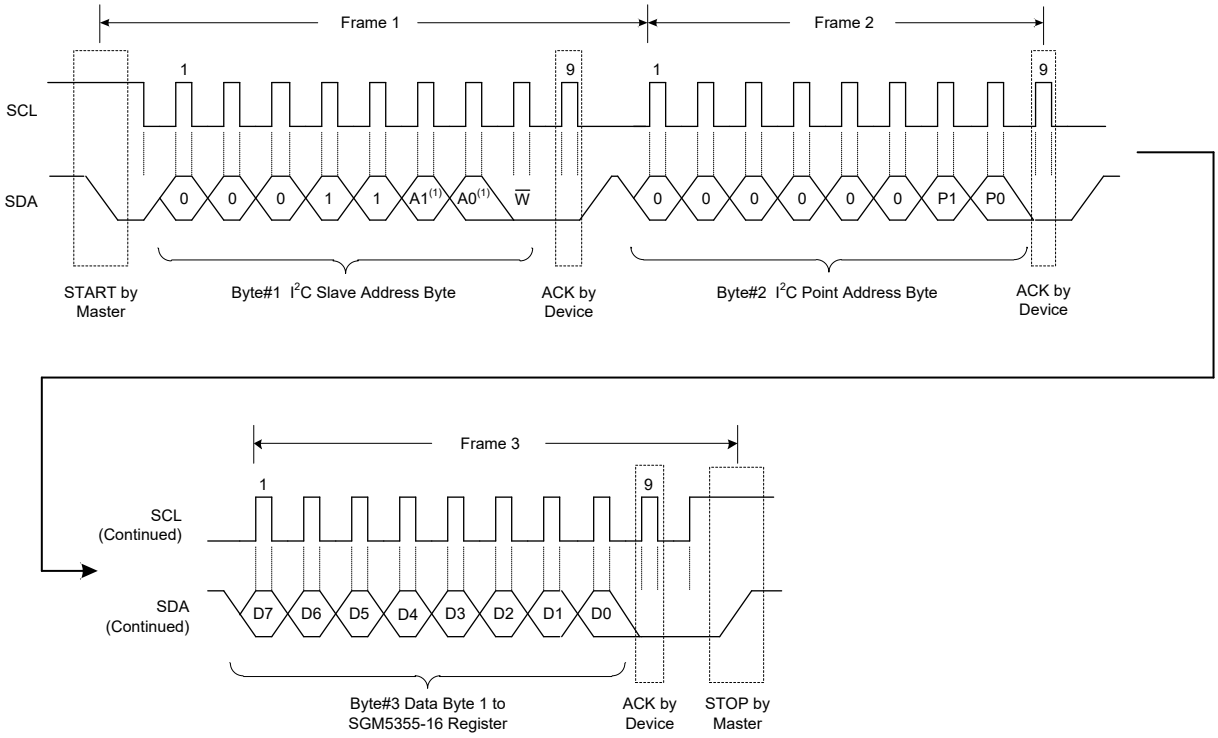
Refer to Figure 4 to Figure 7 for read and write operation demo timing sequences.

All operations must be compatible with I²C protocol, which need be preceded by a start condition and followed by a stop condition.

DETAILED DESCRIPTION (continued)

For example, writing to point register 0x00 sets the SGM5355-16 to normal mode, please refer to the following order:

1. First byte, 0b0001100 (first 7-bit is I²C address), the 8th bit is read/write bit which is low writing now
2. Second byte, 0b00000000 (points to register 0x00)
3. Third byte, 0b00000000 (value 0x00 is wrote, which means PD[1:0] = 00)



NOTE:

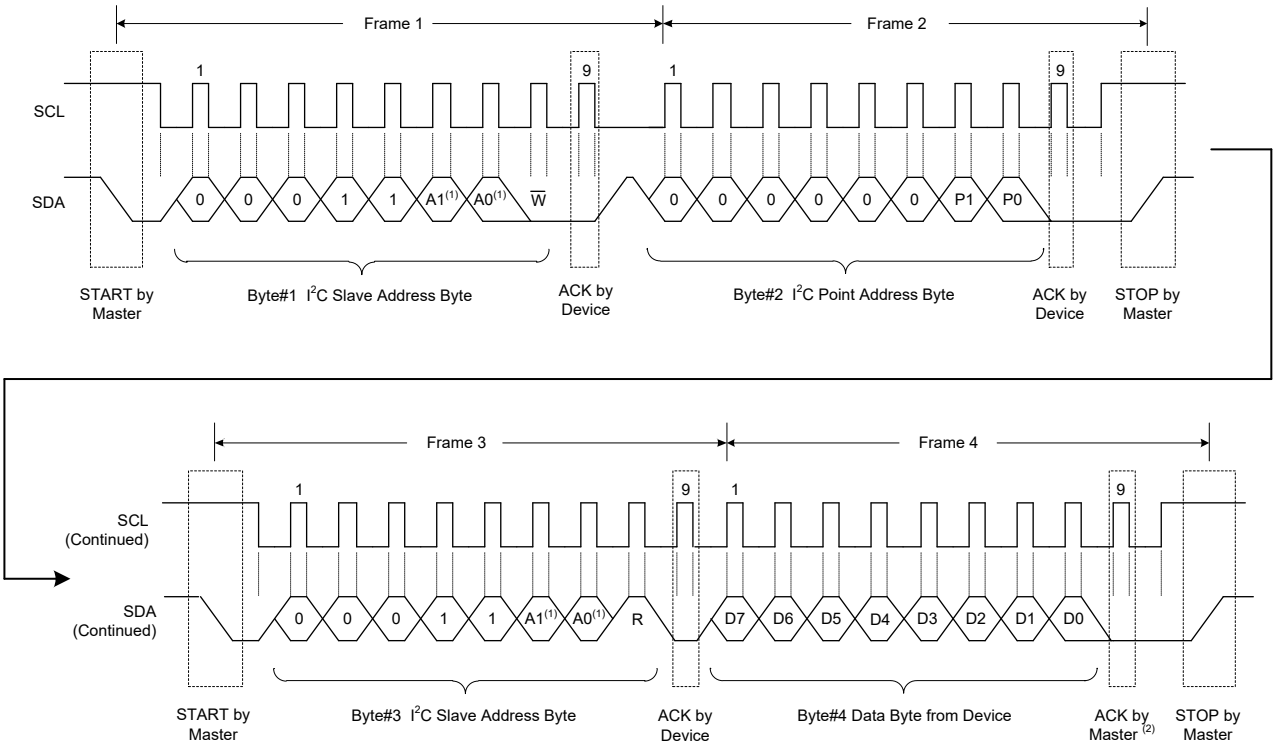
1. The A0 and A1 values depend on the ADDR pin.

Figure 4. Timing Diagram for Write Byte Register

DETAILED DESCRIPTION (continued)

To read from the point register 0x00, please refer to the following order:

1. First byte, 0b0001100 (first 7-bit is I²C address), the 8th bit is read/write bit which is low writing now
2. Second byte, 0b00000000 (points to register 0x00)
3. Third byte, 0b0001101 (first 7-bit is I²C address), the 8th bit is read/write bit which is high reading now
4. Fourth byte, SGM5355-16 answers with 0b000000XX (data of register 0x00)



NOTES:

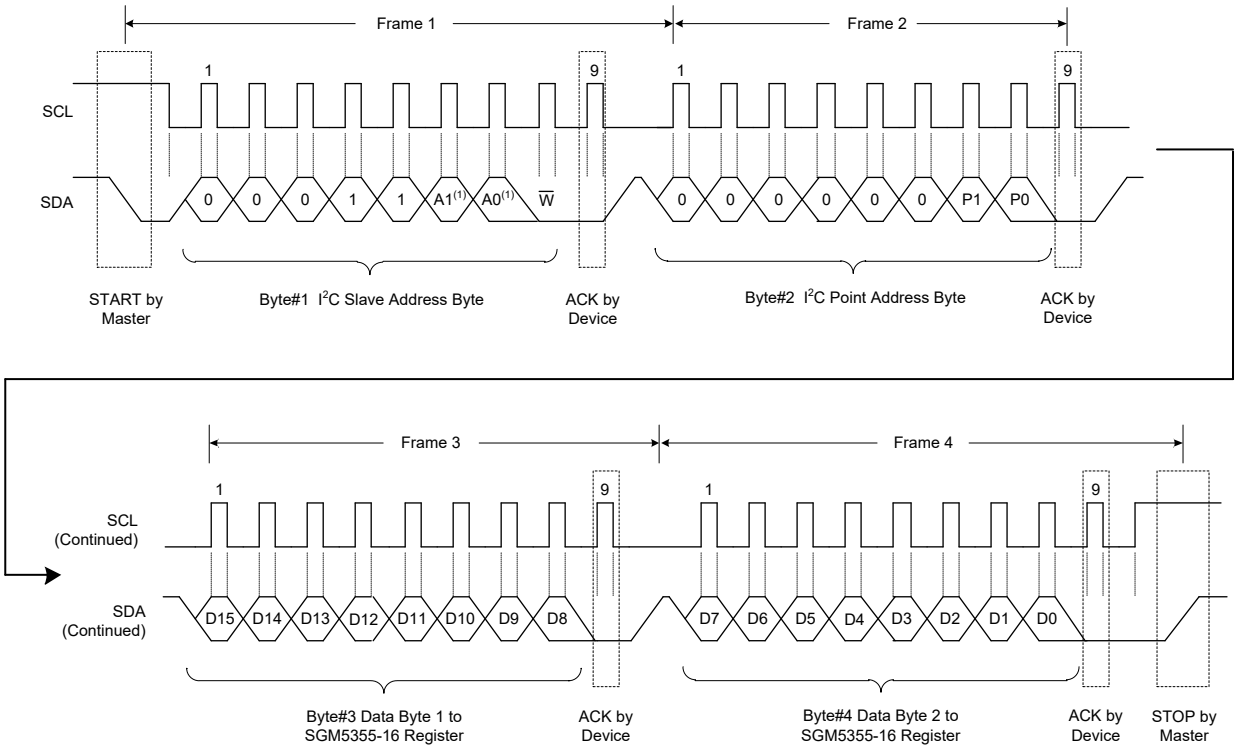
1. The A0 and A1 values depend on the ADDR pin.
2. SDA can be set high by master to terminate a byte read operation.

Figure 5. Timing Diagram for Read Byte Register

DETAILED DESCRIPTION (continued)

To write the output value 0xABCD to point register 0x01, please refer to the following order:

1. First byte, 0b0001100 (first 7-bit is I²C address), the 8th bit is read/write bit which is low writing now
2. Second byte, 0b00000001 (points to register 0x01)
3. Third byte, 0xAB (the high byte 0xAB)
4. Fourth byte, 0xCD (the low byte 0xCD)



NOTE:

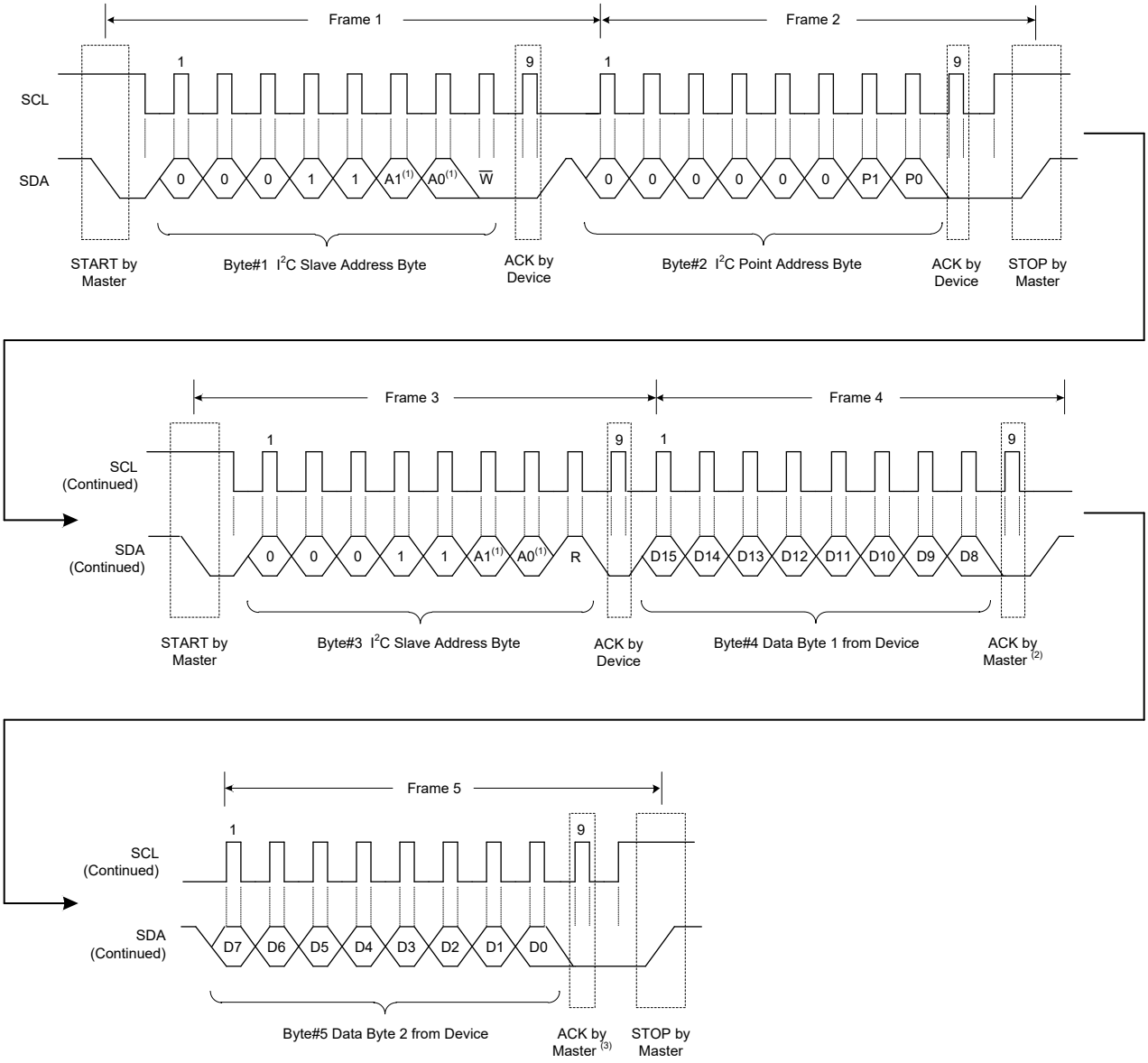
1. The A0 and A1 values depend on the ADDR pin.

Figure 6. Timing Diagram for Write Word Register

DETAILED DESCRIPTION (continued)

To read back the output value 0xABCD from point register 0x01, please refer to the following order:

1. First byte, 0b0001100 (first 7-bit is I²C address), the 8th bit is read/write bit which is low writing now
2. Second byte, 0b00000001 (points to register 0x01)
3. Third byte, 0b0001101 (first 7-bit is I²C address), the 8th bit is read/write bit which is high reading now
4. Fourth byte, SGM5355-16 answers with high byte 0xAB (data of register 0x01 high byte)
5. Fifth byte, SGM5355-16 answers with low byte 0xCD (data of register 0x01 low byte)



NOTES:

1. The A0 and A1 values depend on the ADDR pin.
2. SDA can be set high by master to terminate a single-byte read operation.
3. SDA can be set high by master to terminate a two-byte read operation.

Figure 7. Timing Diagram for Read Word Register

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

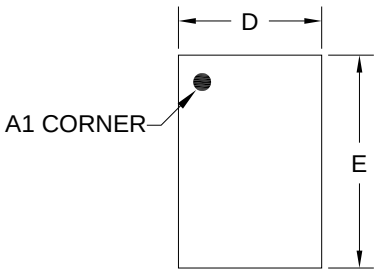
SEPTEMBER 2023 – REV.A.1 to REV.A.2	Page
Updated Detailed Description section	16

JUNE 2022 – REV.A to REV.A.1	Page
Updated Detailed Description section	16

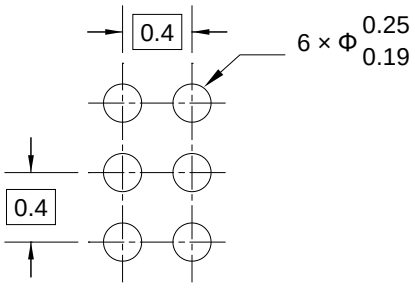
Changes from Original (JANUARY 2022) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

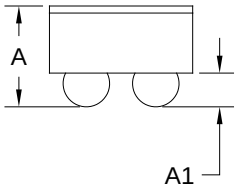
WLCSP-0.82×1.22-6B



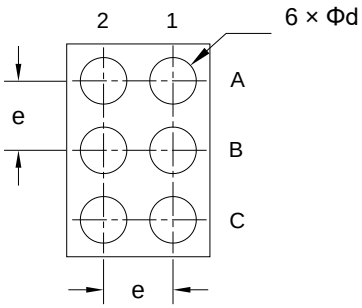
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



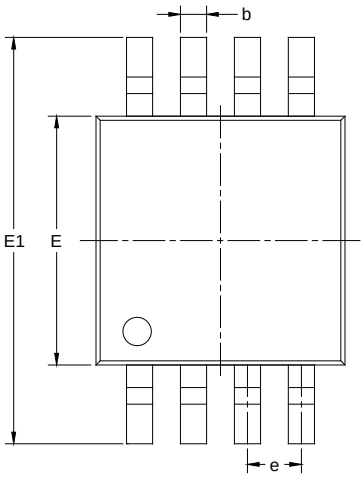
BOTTOM VIEW

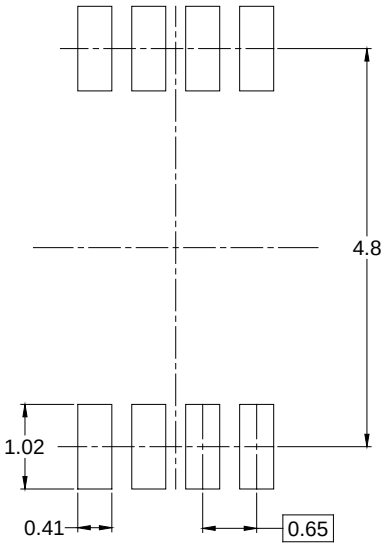
Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.542	0.580	0.618
A1	0.174	0.194	0.214
D	0.800	0.825	0.850
E	1.200	1.225	1.250
d	0.248	0.268	0.288
e	0.400 BSC		

NOTE: This drawing is subject to change without notice.

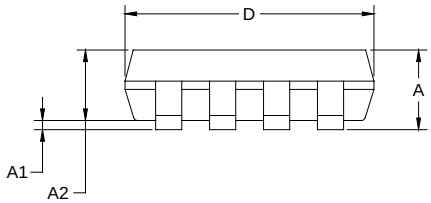
PACKAGE OUTLINE DIMENSIONS

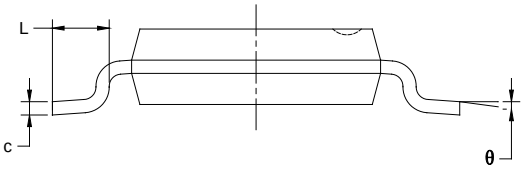
MSOP-8





RECOMMENDED LAND PATTERN (Unit: mm)



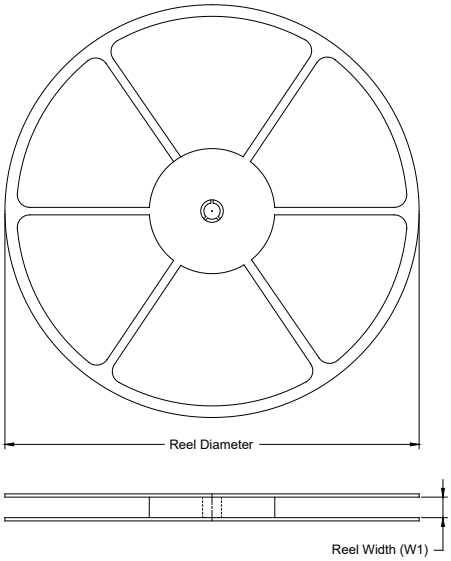


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

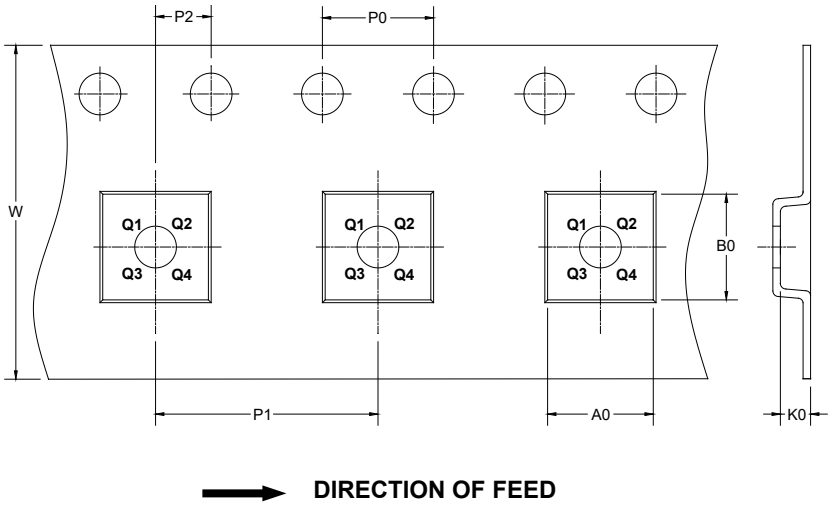
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

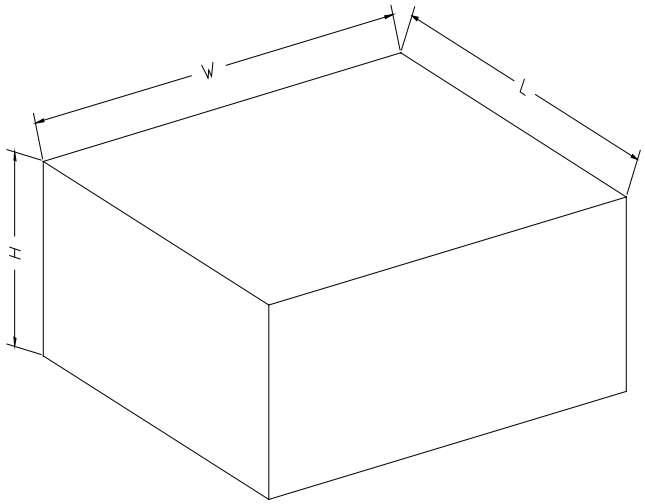
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-0.82×1.22-6B	7″	9.5	0.91	1.31	0.71	4.0	4.0	2.0	8.0	Q1
MSOP-8	13″	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002