SGM42544
Quad Half-Bridge Driver IC

GENERAL DESCRIPTION

The SGM42544 provides four half-bridge drivers, each channel is controlled by separate individually controllable input. It is suitable for driving inductive loads, including four solenoids, relays, DC motors or other loads. The device allows operation with single or bipolar power supplies (such as ±20V).

With proper heatsinking, the SGM42544 can deliver up to 2A peak output current per channel (at T_J = +25℃). Paralleling the outputs is possible for higher current applications.

Protection features include under-voltage lockout, over-current, short-circuit and thermal shutdown. Fault conditions are indicated on the nFAULT pin.

The SGM42544 is available in a Green TSSOP-28 (Exposed Pad) package.

FEATURES

- **Wide Power Supply Voltage Range: 8V to 45V**
- **On-Resistance: 0.44Ω for HS + LS, T_J = +25℃**
- **Flexible Control Interface for Different Loads**
- **Individual Controllable Input**
- **Up to 2A Drive Current at V_M = 24V, T_J = +25℃**
- **Single or Bipolar Power Supplies (up to ±22.5V)**
- **Built-in 3.3V Reference Output**
- **Parallel Digital Control Interface**
- **Full Set of Protections**
  - **V_M Under-Voltage Lockout (UVLO)**
  - **Over-Current Protection (OCP)**
  - **Thermal Shutdown (TSD)**
  - **Fault Condition Indication Pin (nFAULT)**
- **Available in a Green TSSOP-28 (Exposed Pad) Package**

APPLICATIONS

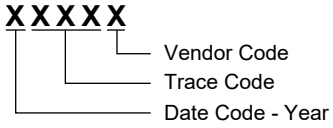
Robotics
Gaming Machines
Factory Automation
Office Automation Machines

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM42544	TSSOP-28 (Exposed Pad)	-40℃ to +125℃	SGM42544XPTS28G/TR	SGM42544 XPTS28 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, V_M ..... -0.3V to 55V
Logic Ground Voltage, LGND ..... -0.5V to V_M - 8V
Digital Pins Voltage Range ..... LGND - 0.5V to LGND + 6V
SRC12, SRC34 (with Optional Sense Resistor) to VNEG Pins ..... -0.7V to 0.7V
Peak Output Current, t < 1μs ..... Internally Limited
Package Thermal Resistance
TSSOP-28 (Exposed Pad), θ_{JA} ..... 27℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage Range, V_M ..... 8V to 45V
V3P3 Load Current ..... 0mA to 10mA
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

DISCLAIMER

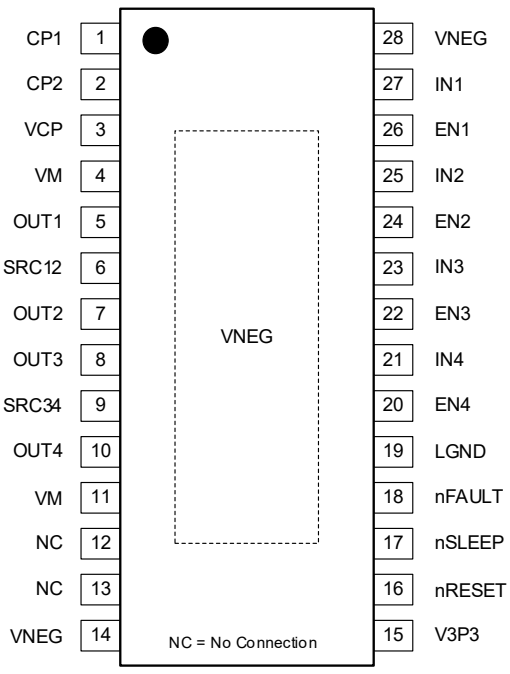
SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

PIN CONFIGURATION

(TOP VIEW)



TSSOP-28 (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	CP1	I/O	Charge Pump Flying Capacitor. A 0.01μF/100V capacitor is used between CP1 and CP2 pins.
2	CP2	I/O	
3	VCP	I/O	Gate Drive Voltage of the High-side Switches. Decouple with a 0.1μF/16V ceramic capacitor to VM pin.
4, 11	VM	-	Power Supply. Connect these pins to the same motor supply (8V to 45V) and bypass with a 100μF (MIN) capacitor.
5	OUT1	O	Output 1 of the Device.
7	OUT2	O	Output 2 of the Device.
8	OUT3	O	Output 3 of the Device.
10	OUT4	O	Output 4 of the Device.
6	SRC12	-	Low-side FET Source for OUT1 and OUT2. Short to VNEG directly or connect an optional sense resistor to VNEG.
9	SRC34	-	Low-side FET Source for OUT3 and OUT4. Short to VNEG directly or connect an optional sense resistor to VNEG.
12, 13	NC	-	No Connection.
14, 28	VNEG	-	Negative Power Supply. Connect to LGND for single supply or connect to negative power supply for dual supplies.
15	V3P3	O	3.3V Regulator Output. Bypass with a 0.47μF/6.3V ceramic capacitor to VNEG.
16	nRESET	I	Reset Input. Active-low reset input with weak internal pull-down initializes internal logic and disables half-bridge outputs.
17	nSLEEP	I	Sleep Mode Input. Active-low sleep mode logic input with weak internal pull-down. Apply high to enable device, and low to enter into the low-power sleep mode.
18	nFAULT	OD	Fault Indication Pin. Open-drain output type, logic low when in fault conditions.
19	LGND	-	Logic Input Reference Ground. Connect to logic ground.
20	EN4	I	Enable Input for Channel 4. Active-high enable logic input with weak internal pull-down.
21	IN4	I	Input Power for Channel 4. Internal pull-down.
22	EN3	I	Enable Input for Channel 3. Active-high enable logic input with weak internal pull-down.
23	IN3	I	Input Power for Channel 3. Internal pull-down.
24	EN2	I	Enable Input for Channel 2. Active-high enable logic input with weak internal pull-down.
25	IN2	I	Input Power for Channel 2. Internal pull-down.
26	EN1	I	Enable Input for Channel 1. Active-high enable logic input with weak internal pull-down.
27	IN1	I	Input Power for Channel 1. Internal pull-down.
Exposed Pad	VNEG	-	Exposed Pad. Exposed pad for thermal dissipation, connect to VNEG.

NOTE: I = input, O = output, OD = open-drain output, I/O = input/output.

ELECTRICAL CHARACTERISTICS

(T_J = +25℃, all voltages relative to VNEG terminal, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
Motor Power Supply Voltage	V_M		8		45	V
Operating Supply Current	I_{VM}	V_M = 24V		2	5	mA
Sleep Mode Supply Current	I_{VMQ}	V_M = 24V		1	2	μA
VM Under-Voltage Lockout Threshold	V_{UVLO}	V_M rising		7.7	7.98	V
V3P3 Regulator						
V3P3 Voltage	V_{V3P3}	I_{OUT} = 0mA to 10mA	3.1	3.3	3.5	V
Logic-Level Inputs						
Input Logic Low Voltage	V_{IL}	LGND = 0V, T_J = -40℃ to +125℃			0.5	V
Input Logic High Voltage	V_{IH}	LGND = 0V, T_J = -40℃ to +125℃	2.7			V
Input Hysteresis	V_{HYS}	LGND = 0V		1.2		V
Input Logic Low Current	I_{IL}	V_{IN} = LGND = 0V	-10		10	μA
Input Logic High Current	I_{IH}	V_{IN} = LGND + 3.3V (LGND = 0V)			50	μA
Internal Pull-Down Resistance	R_{PD}			300		kΩ
nFAULT Output (Open-Drain Output)						
Output Low Voltage	V_{OL}	I_{OUT} = 5mA			0.5	V
Output High Leakage Current	I_{OH}	V_{OUT} = LGND + 3.3V			1	μA
H-Bridge FETs						
HS FET On-Resistance	R_{DSON}	V_M = 24V, I_{OUT} = 1A, T_J = +25℃		0.22		Ω
		V_M = 24V, I_{OUT} = 1A, T_J = +125℃		0.32	0.36	
LS FET On-Resistance		V_M = 24V, I_{OUT} = 1A, T_J = +25℃		0.22		
		V_M = 24V, I_{OUT} = 1A, T_J = +125℃		0.30	0.33	
Protection Circuits						
Over-Current Protection Trip Level	I_{OCP}			3.5		A
Output Dead Time	t_{DEAD}			400		ns
Over-Current Protection Deglitch Time	t_{OCP}			2		μs
Thermal Shutdown Temperature	T_{TSD}	Die temperature		160		℃

SWITCHING CHARACTERISTICS

(T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Delay Time	t_1	ENx high to OUTx high, INx = 1	540		1650	ns
	t_2	ENx low to OUTx low, INx = 1	790		1900	ns
	t_3	ENx high to OUTx low, INx = 0	1020		2120	ns
	t_4	ENx low to OUTx high, INx = 0	690		1900	ns
	t_5	INx high to OUTx high	820		1950	ns
	t_6	INx low to OUTx low	1200		2330	ns
Output Rise Time	t_R	Resistor to VNEG	100		220	ns
Output Fall Time	t_F	Resistor to VNEG	300		670	ns

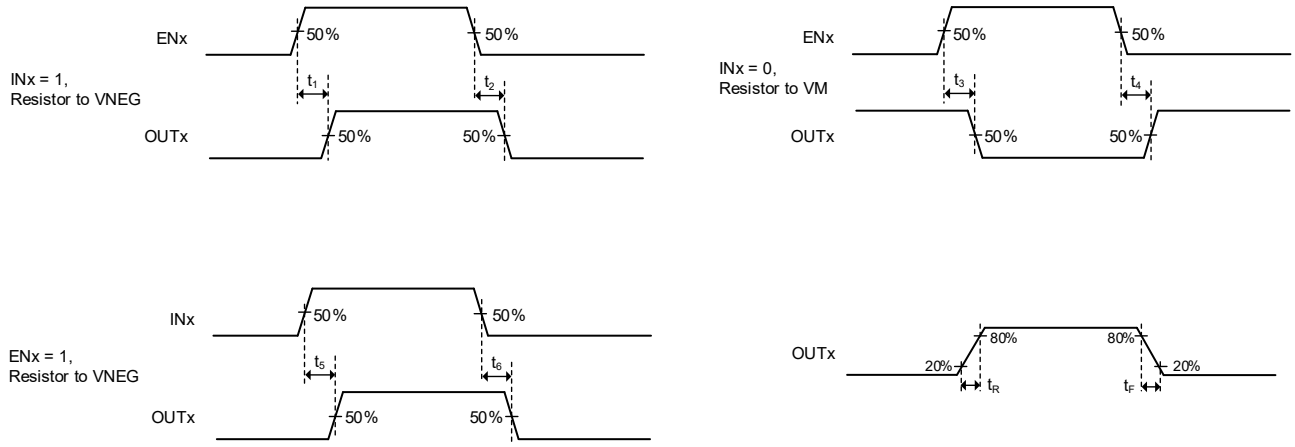
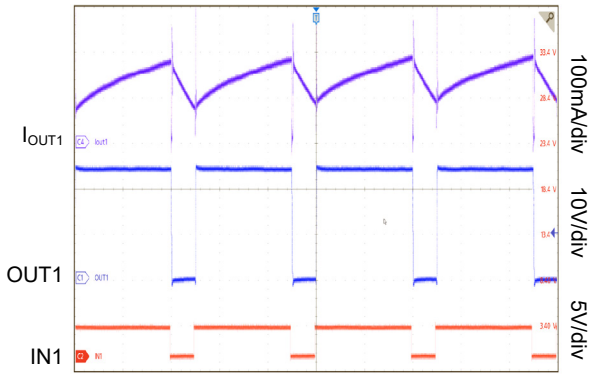


Figure 1. Timing Definitions

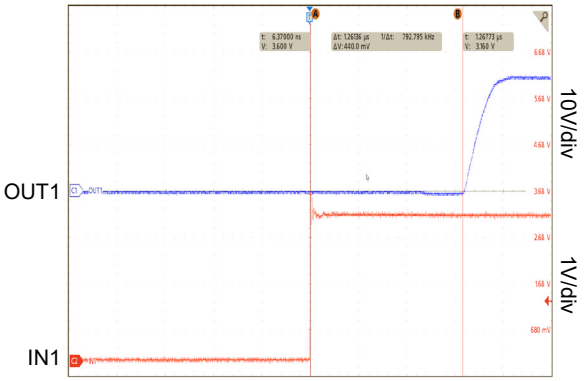
TYPICAL PERFORMANCE CHARACTERISTICS

DC Motor with PWM (80% Duty Cycle)



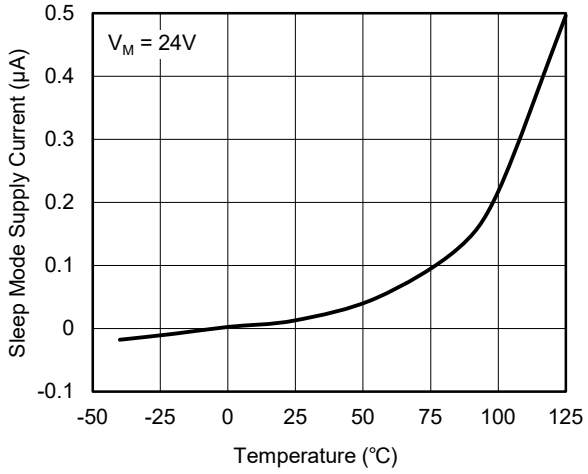
Time (40μs/div)

IN1 to OUT1 Propagation Delay

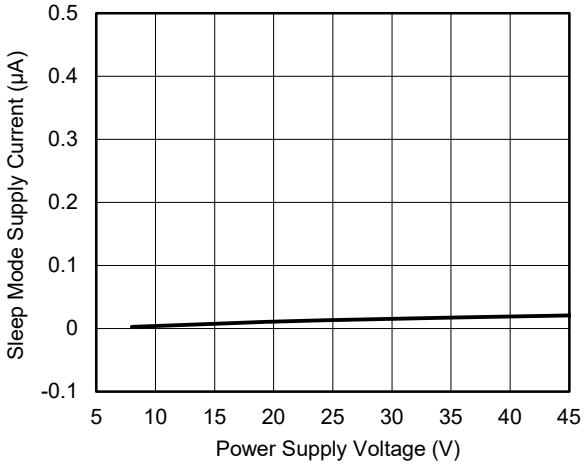


Time (400ns/div)

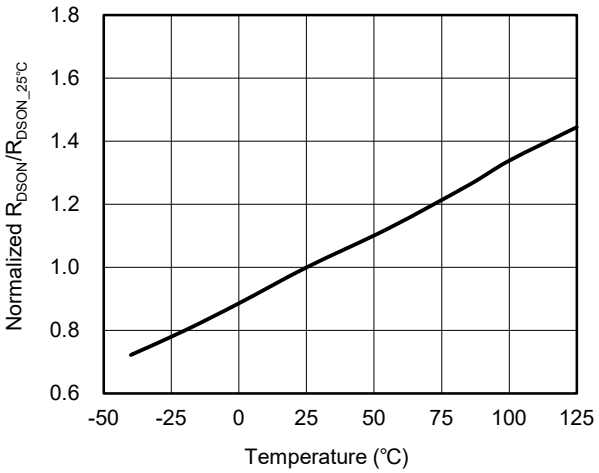
Sleep Mode Supply Current vs. Temperature



Sleep Mode Supply Current vs. Power Supply Voltage



R_{DSON} vs. Temperature



FUNCTIONAL BLOCK DIAGRAM

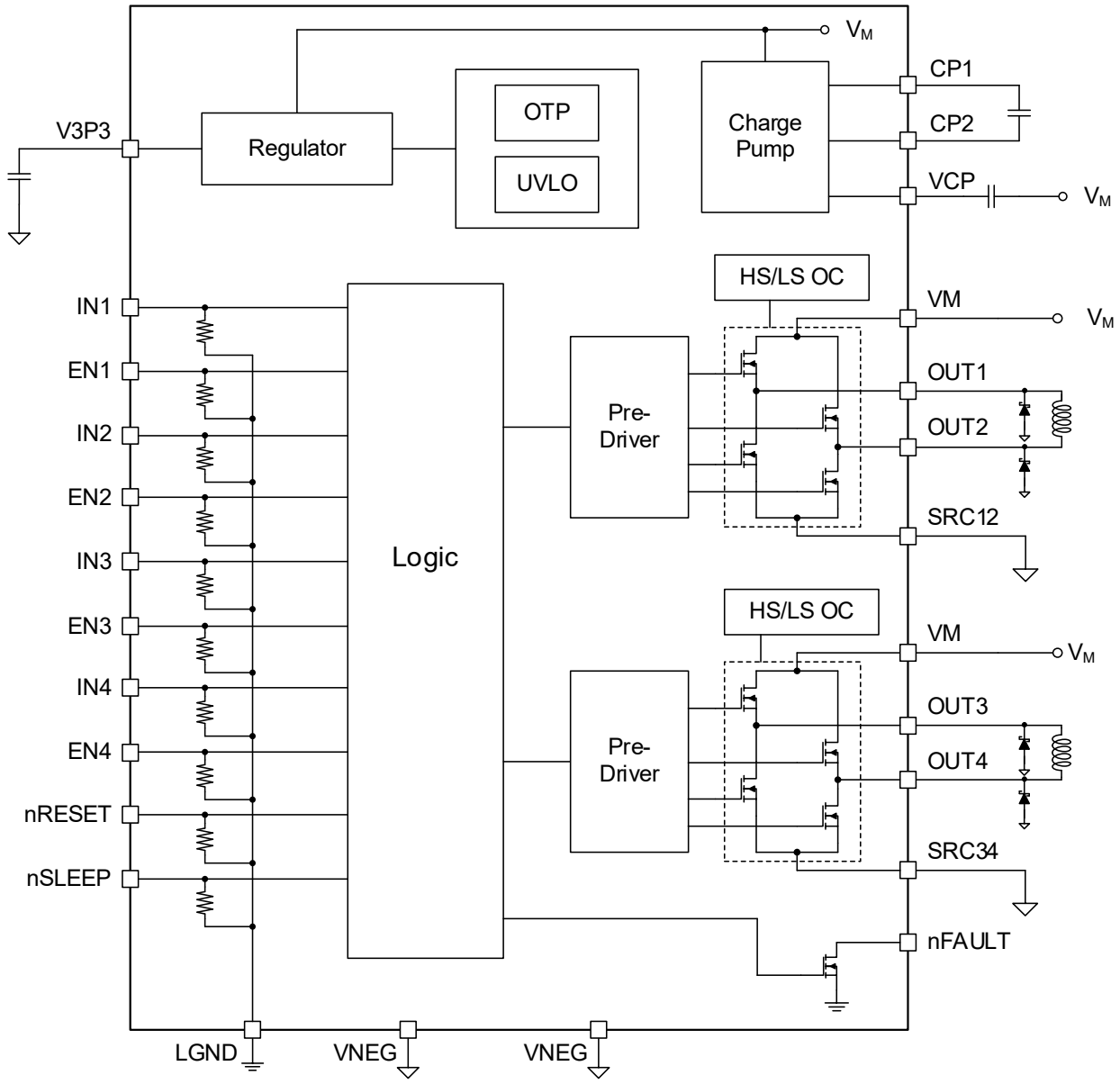


Figure 2. Functional Block Diagram

DETAILED DESCRIPTION

The SGM42544 provides four half-bridge drivers, each channel is controlled by separate individually controllable input. It is suitable for driving inductive loads, including four solenoids, relays, DC motors or other inductive loads. The device allow operation with single or bipolar power supplies, such as ±20V.

Logic Inputs

LGND is the ground reference for all logic input (ENx, INx, nRESET, nSLEEP) and nFAULT signal, it is connected to the microcontroller ground.

Output Stage

The OUTx are driven between VM and VNEG pins. Please refer to the functional block diagram.

Charge Pump

The charge pump is used to generate a gate supply greater than V_M to turn on the high-side MOSFET. A 0.01μF ceramic capacitor is required between CP1 and CP2, and a 0.1μF ceramic capacitor is required between VCP and VM.

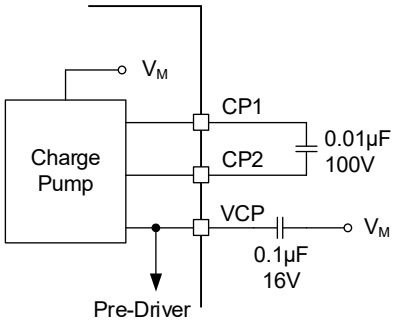


Figure 3. Charge Pump

Bridge Control

For the SGM42544, control of the outputs is accomplished through the INx and ENx. Table 1 shows the logic.

Table 1. H-Bridge Logic

INx	ENx	OUTx
X	0	Z
0	1	L
1	1	H

For DC motors, speed control is typically performed by providing an external PWM signal to the INx or ENx input pins.

Table 2. PWM Function

IN1	EN1	IN2	EN2	FUNCTION
PWM	1	0	1	Forward PWM, Slow Decay
0	1	PWM	1	Reverse PWM, Slow Decay
1	PWM	0	PWM	Forward PWM, Fast Decay
0	PWM	1	PWM	Reverse PWM, Fast Decay

Figure 4 shows the current paths in different drive and decay modes:

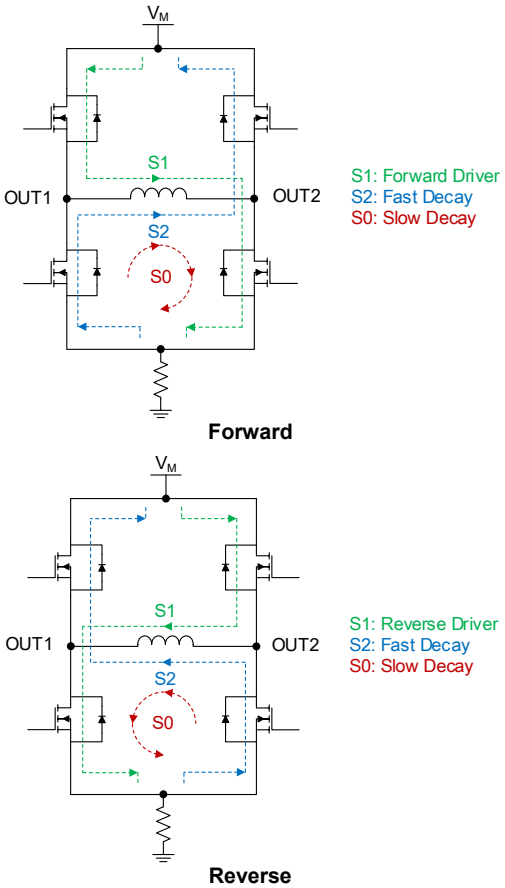


Figure 4. Current Paths

DETAILED DESCRIPTION (continued)

Protection Circuits

The SGM42544 integrated internal circuit protections include thermal shutdown, under-voltage lockout (UVLO), and over-current protection.

Over-Current Protection (OCP)

Each MOSFET is protected by its own preset over-current limit. In case of an over-current (any direction), the whole bridge will be disabled (shutdown), the nFAULT pin will be driven low. An over-current will occur due to a short between a switching node and ground or to the VM supply line, or to the other node of the bridge (a winding short).

If the current limit persists for a period which is longer than the OCP time, all H-bridge MOSFETs will be disabled and the nFAULT pin will be driven low. The device will not restart automatically and will be disabled until V_M supply is removed and re-applied or reset through nRESET pin.

Thermal Shutdown (TSD)

All bridges and drivers are shutdown if a junction over-temperature occurs in the device and the nFAULT pin will be driven low. Once the temperature goes back to the safe level, device resumes its operation.

Under-Voltage Lockout (UVLO)

If the voltages on VM pin fall below their under-voltage lockout threshold, the device will be disabled, internal logic will be reset. Device resumes operation when all of them go back above their UVLO threshold.

nRESET and nSLEEP Operation

This active-low input is used to minimize power consumption when the device is not in use. Sleep mode disables all the internal circuitry, including the output MOSFET, charge pump and regulator. A logic-high allows normal operation, 1.2ms delay is required before output transition.

APPLICATION INFORMATION

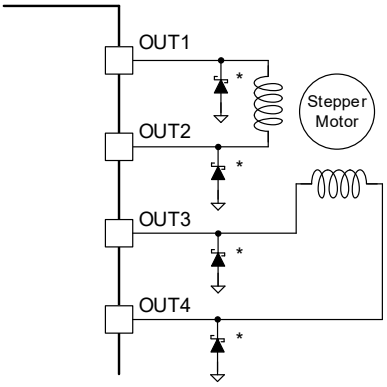


Figure 5. Driving Bipolar Stepper Motor

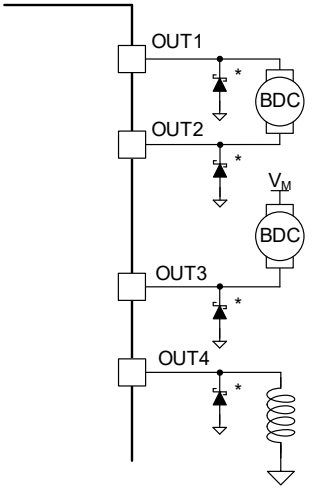


Figure 6. Example Showing Driving Two BDC Motors and One Inductive Load

NOTE: *. The Schottky diode selection depends on customer's application requirements. For example, for 36V/2A application, the Schottky diode selection refers to PMEG4030.

Design Requirements

For the control logic, please refer to the following truth tables:

Table 3. Brushed DC Motor

FUNCTION	EN1	EN2	IN1	IN2	OUT1	OUT2
Forward	1	1	PWM	0	H	L
Reverse	1	1	0	PWM	L	H
Brake	1	1	0	0	L	L
Brake	1	1	1	1	H	H
Coast	0	X	X	X	Z	X
Coast	X	0	X	X	X	Z

Table 4. Single-Direction Brushed DC Motor

FUNCTION	EN3	IN3	OUT3
On	1	nPWM	L
Brake	1	1	H
Coast	0	X	Z

Table 5. Inductive Loads

FUNCTION	EN4	IN4	OUT4
On	1	PWM	H
Off or Slow Decay	1	0	L
Off or Coast	0	X	Z

Paralleling the outputs is possible for higher current applications. If the SGM42544 is intended to be used as two individual half-bridge, OUT1 and OUT2 should be parallel, and OUT3 and OUT4 should be parallel. If configuring the device as H-bridge, paralleling any two outputs will be fine.

APPLICATION INFORMATION (continued)

Bulk Capacitance

To achieve small voltage ripple and decouple the impact of supply line inductances from interfering with the system operation, the bulk local capacitor near the motor driver is needed (V_M supply) as shown in Figure 7. Also, to decouple switching currents of the H-bridges, small high frequency decoupling capacitor is recommended between VM and GND pins.

To select the local capacitance, several factors should be considered including the following:

- Maximum current needed by the motor.
- Supply capacitance and current sourcing capability.
- Parasitic inductance of supply lines.
- Acceptable voltage ripple.
- Motor parameters and required acceleration.

The power supply inductance causes drops and oscillation on V_M line if the local bulk capacitance is insufficient.

Motor datasheets generally advise for the capacitance value, however it is recommended to do a system level test to size the bulk capacitors properly.

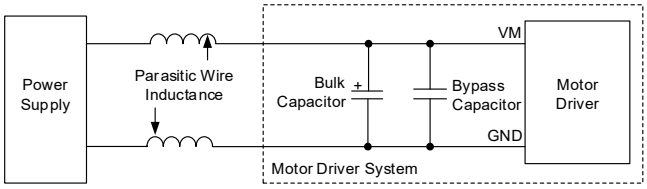


Figure 7. Example Setup of Motor Drive System with External Power Supply

Capacitor voltage rating should be considered well higher than the operating voltage to provide enough margin when the energy transfer is reversed from motor windings back to the V_M supply line and they get charged by the driver.

Layout Guidelines

The PCB should have a thick ground plane. For optimum electrical and thermal performance, the SGM42544 must be soldered directly onto the board. On the underside of the SGM42544 package is an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad must be soldered directly to an exposed surface on the PCB in order to achieve optimal thermal conduction. Thermal vias are used to transfer heat to other layers of the PCB.

The load supply pin (VM) should be decoupled with an electrolytic capacitor in parallel with a lower valued ceramic capacitor placed as close as practicable to the device.

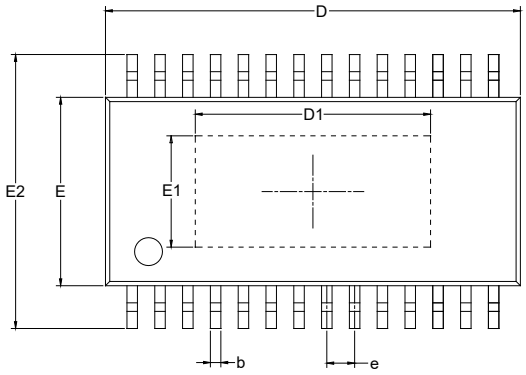
REVISION HISTORY

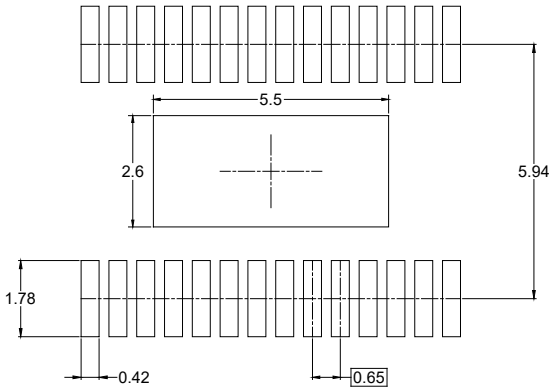
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (SEPTEMBER 2023) to REV.A	Page
Changed from product preview to production data	All

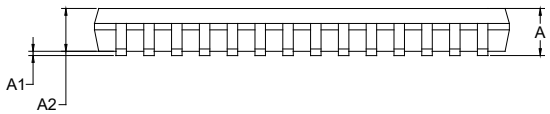
PACKAGE OUTLINE DIMENSIONS

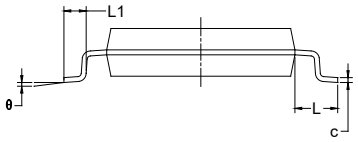
TSSOP-28 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)





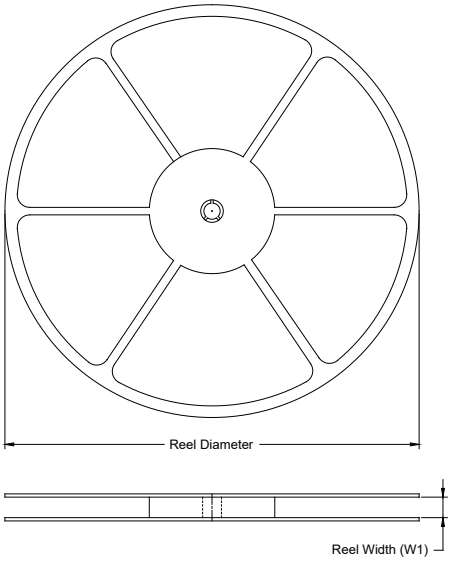
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
D1	5.300	5.700	0.209	0.224
E	4.300	4.500	0.169	0.177
E1	2.400	2.800	0.094	0.110
E2	6.200	6.600	0.244	0.260
e	0.650 BSC		0.026 BSC	
L	1.000 BSC		0.039 BSC	
L1	0.450	0.750	0.018	0.030
θ	0°	8°	0°	8°

NOTES:

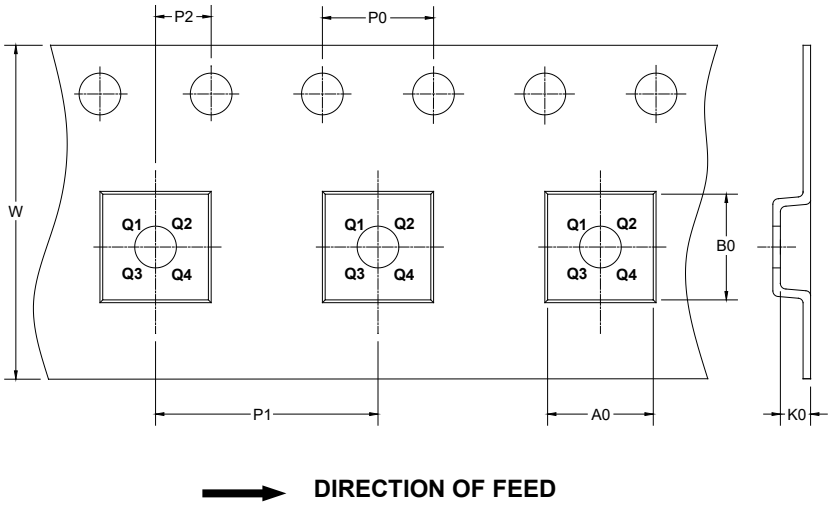
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-153.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

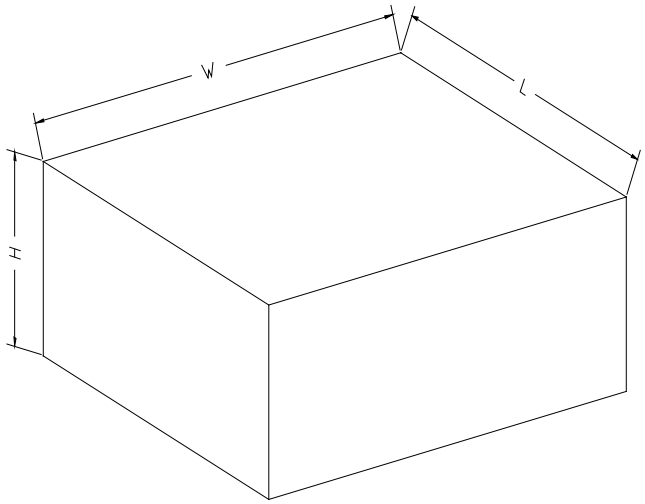
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-28 (Exposed Pad)	13″	16.4	6.80	10.25	1.60	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002