SGM51613H/SGM51652H/SGM51622H 16-Bit, High-Speed, Programmable Bipolar Input Ranges, SAR ADC

GENERAL DESCRIPTION

The SGM51613H, SGM51652H, and SGM51622H are a series of high-precision successive approximation (SAR) analog-to-digital converters (ADCs).

These ADCs are powered by a single unipolar 5V, and support true bipolar ±10.24V, ±5.12V, and ±2.56V inputs, as well as unipolar input ranges of 0V to 10.24V and 0V to 5.12V. The input range is configured by software.

These chips provide over-voltage protection at input, which is up to ±20V.

These chips have an on-chip high accuracy and low drift 10ppm reference.

The input impedance of these chips is ~1MΩ and it is independent of the input range selection.

The digital interface is compatible to the traditional SPI protocol.

The SGM51613H, SGM51652H, and SGM51622H are available in Green TSSOP-16 and TQFN-4×4-16L packages. They are all specified from -40℃ to +125℃.

APPLICATIONS

PLC/DCS Analog Input Modules
Battery Monitoring System
Test and Measurement

FEATURES

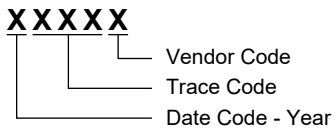
- **16 Bits ADC:**
  - **SGM51613H: 800kSPS**
  - **SGM51652H: 500kSPS**
  - **SGM51622H: 250kSPS**
- **Supported Input Ranges:**
  - **Bipolar Single-Ended Ranges: ±10.24V, ±5.12V, and ±2.56V**
  - **Unipolar Single-Ended Ranges: 0V to 10.24V and 0V to 5.12V**
  - **Bipolar Differential Ranges: ±10.24V, ±5.12V, and ±2.56V**
- **Supply Voltage Ranges:**
  - **Analog Supply: 5V**
  - **I/O Supply: 1.65V to 5V**
- **On-Chip Reference: 4.096V**
- **Differential Nonlinearity (DNL):**
  - **SGM51622H/SGM51652H:**
    -0.55LSB/+0.75LSB (TYP) for All Bipolar Ranges
    -0.7LSB/+1.2LSB (TYP) for All Unipolar Range
  - **SGM51613H:**
    -0.6LSB/+0.75LSB (TYP) for All Bipolar Ranges
    -0.7LSB/+1.4LSB (TYP) for All Unipolar Range
- **Integral Nonlinearity (INL):**
  - **SGM51622H/SGM51652H:**
    ±1LSB (TYP) for All Bipolar Ranges
    ±1.5LSB (TYP) for All Unipolar Range
  - **SGM51613H:**
    ±1.5LSB (TYP) for All Bipolar Ranges
    ±2LSB (TYP) for All Unipolar Range
- **Signal-to-Noise Ratio (SNR):**
  - **SGM51622H/SGM51652H: 91dB (TYP)**
  - **SGM51613H: 90.5dB (TYP)**
- **Total Harmonic Distortion (THD):**
  - **SGM51622H/SGM51652H: -104dB (TYP)**
  - **SGM51613H: -100dB (TYP)**
- **Alarm Features**
- **Daisy-Chain Operation**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green TSSOP-16 and TQFN-4×4-16L Packages**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM51613H	TSSOP-16	-40℃ to +125℃	SGM51613HXTS16G/TR	SGM01A XTS16 XXXXX	Tape and Reel, 4000
	TQFN-4×4-16L	-40℃ to +125℃	SGM51613HXTQE16G/TR	SGM01B XTQE16 XXXXX	Tape and Reel, 3000
SGM51652H	TSSOP-16	-40℃ to +125℃	SGM51652HXTS16G-S/TR	SGM018 XTS16 XXXXX	Tape and Reel, 500
			SGM51652HXTS16G/TR	SGM018 XTS16 XXXXX	Tape and Reel, 4000
	TQFN-4×4-16L	-40℃ to +125℃	SGM51652HXTQE16G/TR	SGM019 XTQE16 XXXXX	Tape and Reel, 3000
SGM51622H	TSSOP-16	-40℃ to +125℃	SGM51622HXTS16G/TR	SGM01C XTS16 XXXXX	Tape and Reel, 4000
	TQFN-4×4-16L	-40℃ to +125℃	SGM51622HXTQE16G/TR	SGM01D XTQE16 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

AIN_P, AIN_N to AGND (AVDD = 5V) ..... -20V to 20V
AIN_P, AIN_N to AGND (AVDD = Floating) ..... -11V to 11V
AVDD to AGND ..... -0.3V to 6V
DVDD to DGND ..... -0.3V to AVDD
Digital Input Pins Voltage Range ..... -0.3V to DVDD + 0.3V
Digital Output Pins Voltage Range ..... -0.3V to DVDD + 0.3V
REFCAP to REFGND ..... -0.3V to 5.7V
REFIO to REFGND ..... -0.3V to 5.7V
REFGND to AGND ..... -0.3V to 0.3V
AGND to DGND ..... -0.3V to 0.3V
Package Thermal Resistance
TSSOP-16, θ_{JA} ..... 125℃/W
TQFN-4×4-16L, θ_{JA} ..... 40℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM (Analog Input Pins: AIN_P, AIN_N) 7000V
HBM (Other Pins) 4000V
CDM 500V

RECOMMENDED OPERATING CONDITIONS

Analog Supply Voltage, AVDD ..... 4.75V to 5.25V, 5V (TYP)
Digital Supply Voltage, DVDD ..... 1.65 to AVDD, 3.3V (TYP)
Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

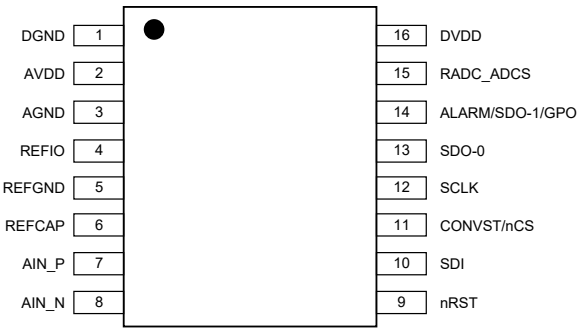
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

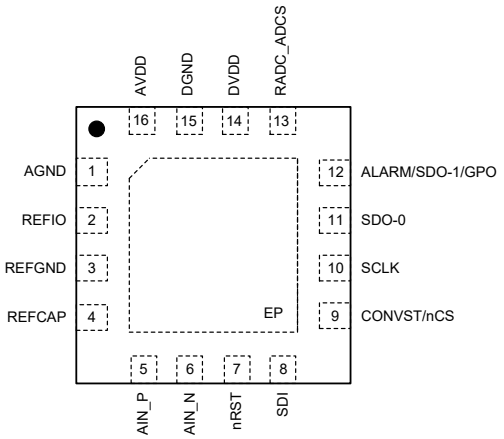
PIN CONFIGURATIONS

(TOP VIEW)



TSSOP-16

(TOP VIEW)



TQFN-4×4-16L

PIN DESCRIPTION

PIN		NAME	TYPE (1)	FUNCTION
TSSOP-16	TQFN-4×4-16L			
1	15	DGND	P	Digital Ground.
2	16	AVDD	P	Analog Power Supply.
3	1	AGND	P	Analog Ground.
4	2	REFIO	AIO	Internal Reference Output and External Reference Input Pin.
5	3	REFGND	AI	Reference Ground Pin.
6	4	REFCAP	AO	ADC Reference Buffer Decoupling Capacitor Pin.
7	5	AIN_P	AI	Positive Analog Input.
8	6	AIN_N	AI	Negative Analog Input.
9	7	nRST	DI	Logic Input to Reset the Device. Active low.
10	8	SDI	DI	Dual Function: Serial Data Input. Chain data input during the serial communication in daisy-chain mode.
11	9	CONVST/ nCS	DI	Dual-Function Pin. Conversion start input pin, active high. The CONVST rising edge converts the device from the acquisition phase to the conversion phase. Chip-Select Input Pin. Active low. When nCS is high, SDO pin goes to tri-state.
12	10	SCLK	DI	Serial Clock Input.
13	11	SDO-0	DO	Serial Data Output 0.
14	12	ALARM/ SDO-1/GPO	DO	Multi-Function Output Pin. Active high alarm. Serial Data Output 1. General-Purpose Output Pin.
15	13	RADC_ADCS	DO	Multi-Function Output Pin for Serial Interface. See the RESET State section. When nCS remains high, the RADC_ADCS reflects the status of the internal ADCST signal. When nCS goes low, the RADC_ADCS keeps low output during data transfer frame.
16	14	DVDD	P	Digital Power Supply.
–	Exposed Pad	EP	–	Exposed pad should be soldered to PCB board and connected to AGND.

NOTE: 1. AI = Analog Input, DI = Digital Input, DO = Digital Output, AIO = Analog Input/Output, P = Power Supply.

ELECTRICAL CHARACTERISTICS

(AVDD = 5V, DVDD = 3.3V, V_{REF} = 4.096V (internal), and maximum throughput, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Inputs							
Absolute Input Voltage Range	AIN_P-AGND	Input range = ±2.5 × V_{REF}		-10.24		10.24	V
		Input range = ±1.25 × V_{REF}		-5.12		5.12	
		Input range = ±0.625 × V_{REF}		-2.56		2.56	
		Input range = 2.5 × V_{REF} (2)		0		10.24	
		Input range = 1.25 × V_{REF} (2)		0		5.12	
	AIN_N-AGND	Input range = ±2.5 × V_{REF}		-10.24		10.24	V
		Input range = ±1.25 × V_{REF}		-5.12		5.12	
		Input range = ±0.625 × V_{REF}		-2.56		2.56	
		Input range = 2.5 × V_{REF} (2)			0		
		Input range = 1.25 × V_{REF} (2)			0		
Input Voltage Range (1) (Single-Ended Input)	AIN_P-AIN_N (AIN_N = AGND) or AIN_P-AIN_N (AIN_P = AGND)	Input range = ±2.5 × V_{REF}		-10.24		10.24	V
		Input range = ±1.25 × V_{REF}		-5.12		5.12	
		Input range = ±0.625 × V_{REF}		-2.56		2.56	
		Input range = 2.5 × V_{REF} (2)		0		10.24	
		Input range = 1.25 × V_{REF} (2)		0		5.12	
Input Voltage Range (1) (Bipolar Differential Input)	AIN_P-AIN_N	Input range = ±2.5 × V_{REF}		-10.24		10.24	V
		Input range = ±1.25 × V_{REF}		-5.12		5.12	
		Input range = ±0.625 × V_{REF}		-2.56		2.56	
Input Voltage Range (1) (Bipolar Differential Input)	Common Mode Input Range	Input range = ±2.5 × V_{REF} (3)		-5.0		7.5	V
		Input range = ±1.25 × V_{REF} (3)		-2.5		5.0	
		Input range = ±0.625 × V_{REF} (3)		-1.2		2.5	
Input Impedance	R_{IN}				1		MΩ
Input Impedance Drift					15		ppm/°C
Input Current	I_{IN}	With voltage at the AIN_P pin = V_{IN}	V_{IN} = 10.24V		7.3		μA
			V_{IN} = 5.12V		2.8		
			V_{IN} = 2.56V		0.9		
Input Over-Voltage Protection Circuit							
All Input Ranges	V_{OVP}	AVDD = 5V, all input ranges		-20		20	V
		AVDD = floating, all input ranges		-11		11	
Input Bandwidth (If without otherwise noted, the following parameters are tested with single-ended input.)							
Small-Signal Input Bandwidth	f_{-3dB}	All input ranges	-3dB		11.6		kHz
	$f_{-0.1dB}$	All input ranges	-0.1dB		1.9		
System Performance (If without otherwise noted, the following parameters are tested with single-ended input.)							
Resolution						16	Bits
No Missing Codes	NMC			16			Bits
Differential Nonlinearity (4)	DNL	SGM51622H/ SGM51652H	All bipolar ranges (5)	-0.99	-0.55/+0.75	2	LSB
			All unipolar ranges (6)	-0.99	-0.7/+1.2	3	
		SGM51613H	All bipolar ranges (5)	-0.99	-0.6/+0.75	2.5	
			All unipolar ranges (6)	-0.99	-0.7/+1.4	3	

ELECTRICAL CHARACTERISTICS (continued)

(AVDD = 5V, DVDD = 3.3V, V_{REF} = 4.096V (internal), and maximum throughput, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Integral Nonlinearity (4)	INL	SGM51622H/ SGM51652H	All bipolar ranges (5)	-3.8	±1	3.8	LSB
			All unipolar ranges (6)	-10	±1.5	4	
		SGM51613H	All bipolar ranges (5)	-4	±1.5	4	
			All unipolar ranges (6)	-10	±2	4	
Offset Error (7)	E_O	T_A = +25℃	Input range = ±2.5 × V_{REF}	-3	0.47	3	mV
			Input range = ±1.25 × V_{REF}	-2.2	0.34	2.2	
			Input range = ±0.625 × V_{REF}	-2	0.33	2	
			Input range = 2.5 × V_{REF}	-2.5	0.61	2.5	
			Input range = 1.25 × V_{REF}	-2.2	0.41	2.2	
Offset Error Drift with Temperature		All input ranges		-2.3	0.71	2.3	ppm/℃
Gain Error (8)	E_G	T_A = +25℃	Input range = ±2.5 × V_{REF}	-0.06	0.01	0.06	%FSR
			Input range = ±1.25 × V_{REF}	-0.45	0.10	0.45	
			Input range = ±0.625 × V_{REF}	-0.6	0.16	0.6	
			Input range = 2.5 × V_{REF}	-0.06	0.01	0.06	
			Input range = 1.25 × V_{REF}	-0.45	0.10	0.45	
Gain Error Drift with Temperature (9)		All input ranges		-5.4	2.4	5.4	ppm/℃
Dynamic Characteristics (If without otherwise noted, the following parameters are tested with single-ended input.)							
Signal-to-Noise Ratio (10)	SNR	SGM51613H	Input range = ±2.5 × V_{REF}	87.4	90.5		dB
			Input range = ±1.25 × V_{REF}	87.2	90		
			Input range = ±0.625 × V_{REF}	86.7	89.5		
			Input range = 2.5 × V_{REF}	83.2	85		
			Input range = 1.25 × V_{REF}	83	85		
		SGM51622H/ SGM51652H	Input range = ±2.5 × V_{REF}	87.8	91		
			Input range = ±1.25 × V_{REF}	87.6	90.5		
			Input range = ±0.625 × V_{REF}	87	90		
			Input range = 2.5 × V_{REF}	83.5	85		
			Input range = 1.25 × V_{REF}	83.3	85		
Total Harmonic Distortion (10) (11)	THD	SGM51613H	All input ranges		-100		dB
		SGM51622H/ SGM51652H			-104		
Signal-to-Noise + Distortion (10)	SINAD	SGM51613H	Input range = ±2.5 × V_{REF}	87	90.3		dB
			Input range = ±1.25 × V_{REF}	86.6	89.7		
			Input range = ±0.625 × V_{REF}	86.4	89.2		
			Input range = 2.5 × V_{REF}	82.6	84.8		
			Input range = 1.25 × V_{REF}	82.3	84.8		
		SGM51622H/ SGM51652H	Input range = ±2.5 × V_{REF}	87.2	90.7		
			Input range = ±1.25 × V_{REF}	87	89.7		
			Input range = ±0.625 × V_{REF}	86.8	89.2		
			Input range = 2.5 × V_{REF}	83	84.8		
			Input range = 1.25 × V_{REF}	82.5	84.8		

ELECTRICAL CHARACTERISTICS (continued)

(AVDD = 5V, DVDD = 3.3V, V_{REF} = 4.096V (internal), and maximum throughput, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Spurious Free Dynamic Range (10)	SFDR	SGM51613H	All input ranges		104		dB
		SGM51622H/ SGM51652H			108		
Sampling Dynamics							
Conversion Time	t_{CONV}	SGM51613H				950	ns
		SGM51652H				1000	
		SGM51622H				2000	
Acquisition Time	t_{ACQ}	SGM51613H		300			ns
		SGM51652H		1000			
		SGM51622H		2000			
Maximum Throughput Rate without Latency	f_{CYCLE}	SGM51613H				800	kSPS
		SGM51652H				500	
		SGM51622H				250	
Internal Reference Output							
Decoupling Capacitor on REFIO Pin	C_{OUT_REFIO}			0.1			μF
Initial Reference Voltage	V_{REFCAP}	T_A = +25℃		4.092	4.096	4.100	V
REFCAP Temperature Drift					10		ppm/℃
Decoupling Capacitor on REFCAP Pin	C_{OUT_REFCAP}			10			μF
Turn-On Time		C_{OUT_REFCAP} = 10μF, C_{OUT_REFIO} = 0.1μF			50		ms
External Reference Input							
External Reference Voltage on REFIO (12)	V_{REFIO_EXT}	REFIO pin configured as an input		4.046	4.096	4.5	V
AVDD Comparator							
High Threshold Voltage	V_{TH_HIGH}				5.35		V
Low Threshold Voltage	V_{TH_LOW}				4.62		V
Power-Supply Requirements							
Analog Power-Supply Voltage	AVDD			4.75	5	5.25	V
Digital Power-Supply Voltage	DVDD	Operating range		1.65		AVDD	V
		Supply range for specified performance		2.7	3.3	AVDD	
Analog Supply Current, Device Converting at Maximum Throughput	I_{AVDD_DYN}	SGM51622H			4.8	6.8	mA
		SGM51652H			6.3	8.4	
		SGM51613H			7.3	9.4	
Analog Supply Current, Device Not Converting	I_{AVDD_STC}				3.45	5.2	mA
Analog Supply Current, Device in STANDBY Mode	I_{AVDD_STDBY}				1.8		mA
Analog Supply Current, Device in PD Mode	I_{AVDD_PD}				7.5		μA
Digital Supply Current, Maximum Throughput	I_{DVDD_DYN}	SGM51613H/SGM51652H			0.1	0.3	mA
		SGM51622H			0.05	0.2	
Digital Supply Current, Device in STANDBY Mode	I_{DVDD_STDBY}				4		μA
Digital Supply Current, Device in PD Mode	I_{DVDD_PD}				4		μA

ELECTRICAL CHARACTERISTICS (continued)

(AVDD = 5V, DVDD = 3.3V, V_{REF} = 4.096V (internal), and maximum throughput, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Inputs						
Digital High Input Voltage	V_{IH}		0.8 × DVDD		DVDD	V
Digital Low Input Voltage	V_{IL}		0		0.2 × DVDD	V
Input Leakage Current				100		nA
Input Pin Capacitance				5		pF
Digital Outputs						
Digital High Output Voltage	V_{OH}	I_O = 500μA source	DVDD - 0.2		DVDD	V
Digital Low Output Voltage	V_{OL}	I_O = 500μA sink	0		0.2	V
Floating State Leakage Current		Only for digital output pins		100		nA
Internal Pin Capacitance				5		pF
Temperature Range						
Operating Free-Air Temperature	T_A		-40		125	℃

NOTES:

1. Ideal input range. It does not consider gain and offset error.
2. These two unipolar input ranges are only valid for unipolar single-ended input with AIN_N = AGND.
3. The input common mode voltage range is guaranteed by design, and tested by limited samples, and not covered by manufacture testing. When the input common mode voltage exceeds ±100mV, the critical DC and AC performances are not guaranteed.
4. This is best-fit INL.
5. Bipolar ranges are ±10.24V, ±5.12V, and ±2.56V, only tested in singled-ended input.
6. Unipolar ranges are 0V to 10.24V and 0V to 5.12V, only tested in singled-ended input.
7. Measured relative to actual measured reference.
8. Excludes internal reference accuracy error.
9. Excludes internal reference temperature drift.
10. All specifications expressed in decibels (dB) refer to the full-scale input (FSR) and are tested with a 1kHz input signal 0.25dB below full-scale, unless otherwise specified.
11. Calculated on the first nine harmonics of the input frequency.
12. Extended functional range limits are set by sample characterization across the temperature range.

TIMING CHARACTERISTICS

(AVDD = 5V, DVDD = 3.3V, V_{REF} = 4.096V (internal), and maximum throughput, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Cycle						
Sampling Frequency	f_{CYCLE}	SGM51613H			800	kSPS
		SGM51652H			500	
		SGM51622H			250	
ADC Cycle Time Period	t_1		$1/f_{CYCLE}$			
Acquisition Time	t_{ACQ}	SGM51613H	300			ns
		SGM51652H	1000			
		SGM51622H	2000			
Conversion Time	t_{CONV}	SGM51613H			950	ns
		SGM51652H			1000	
		SGM51622H			2000	
Asynchronous Reset						
Pulse Duration	t_2	nRST low	100			ns
		nRST low in PD mode	50			μs
Delay Time for POR Reset	t_3			100		ns
Delay Time for Application Reset	t_{14}	nRST rising to CONVST/nCS rising		100		ns
Wake-Up Time	t_{NAP_WKUP}	NAP mode		10		μs
Power-Up Time	t_{PWRUP}	PD mode		0.3		ms
SPI-Compatible Serial Interface						
Serial Clock Frequency	f_{CLK}				40	MHz
Serial Clock Time Period	t_{CLK}		$1/f_{CLK}$			
SCLK High Time	t_{15}		0.45		0.55	t_{CLK}
SCLK Low Time	t_{16}		0.45		0.55	t_{CLK}
Setup Time: CONVST/nCS Falling to First SCLK Capture Edge	t_7		8			ns
Setup Time: SDI Data Valid to SCLK Capture Edge	t_{12}		8			ns
Hold Time: SCLK Capture Edge to (Previous) Data Valid on SDI	t_{13}		8			ns
Delay Time: Last SCLK Capture Edge to CONVST/nCS Rising	t_8		8			ns
Delay Time: CONVST/nCS Falling Edge to Data Enable	t_9				10	ns
Delay Time: CONVST/nCS Rising to SDO-x Going to 3-State	t_{11}				10	ns
Delay Time: SCLK Launch Edge to (Next) Data Valid on SDO-x	t_{10}				12	ns
Delay Time: CONVST/nCS Rising Edge to RVS Falling	t_6				15	ns

NOTE: SGM51613H only supports the SPI-compatible protocols with dual SDO-x.

TIMING DIAGRAM

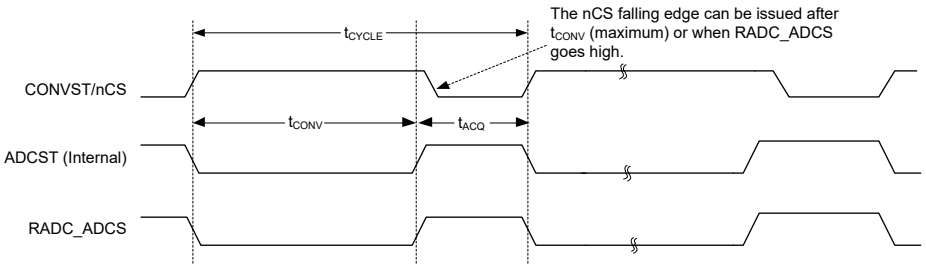


Figure 1. Conversion Cycle Timing Diagram

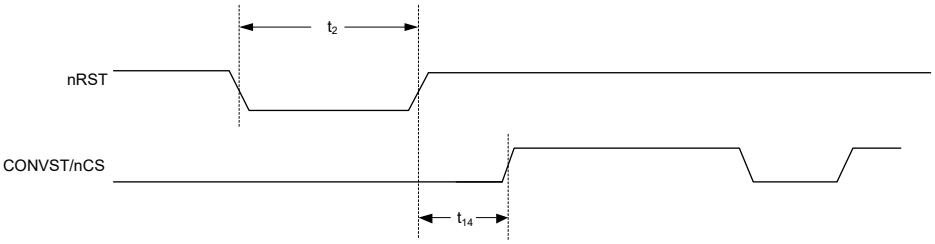
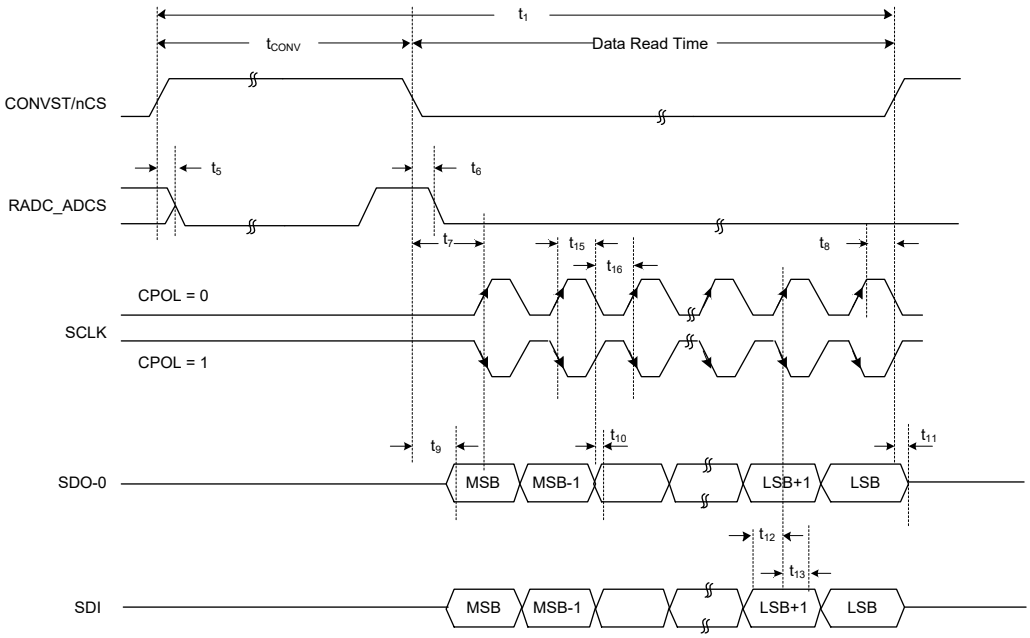


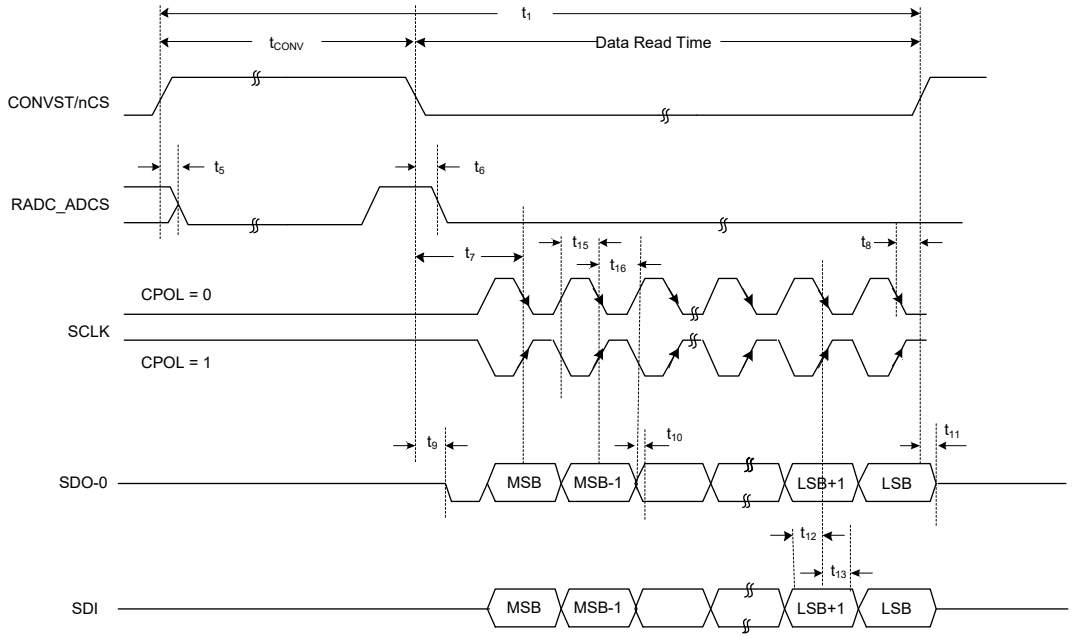
Figure 2. Asynchronous Reset Timing Diagram



NOTE: On SDI pin, the chip counts the last valid data bit as LSB before the nCS rising edge, and accepts the according data bits from LSB to MSB.

Figure 3. Standard SPI Interface Timing Diagram (CPHA = 0)

TIMING DIAGRAM (continued)

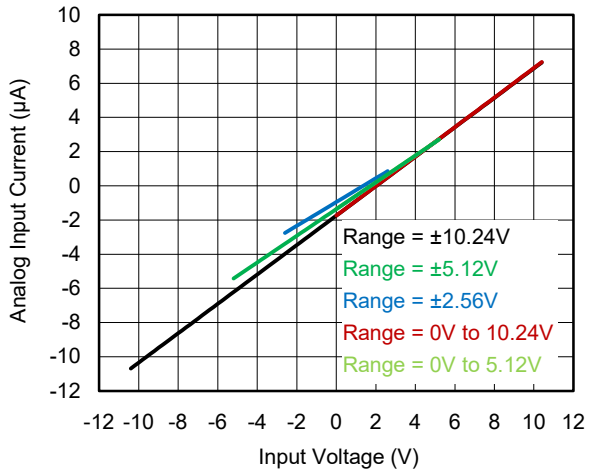


NOTE: On SDI pin, the chip counts the last valid data bit as LSB before the nCS rising edge, and accepts the according data bits from LSB to MSB.

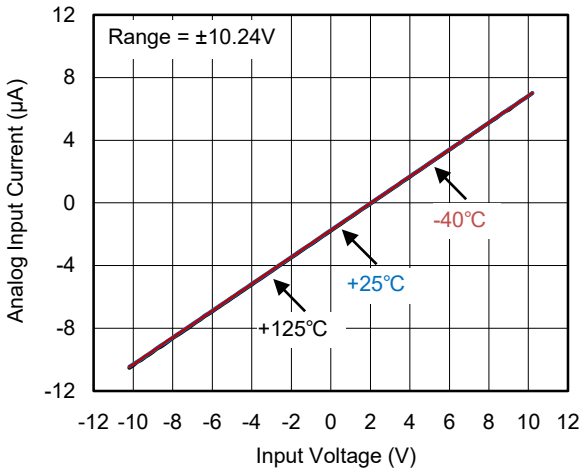
Figure 4. Standard SPI Interface Timing Diagram (CPHA = 1)

TYPICAL PERFORMANCE CHARACTERISTICS

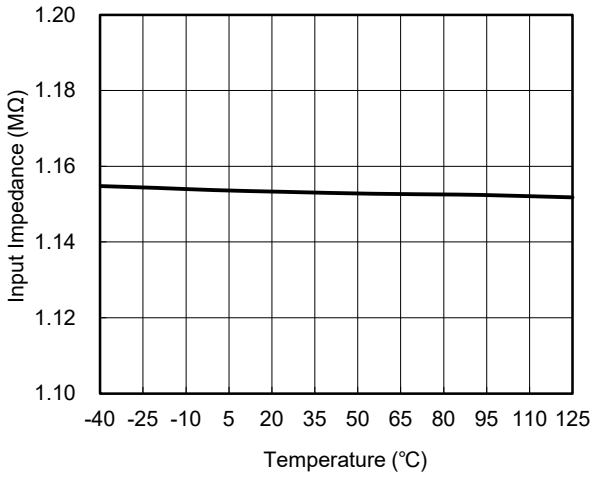
Input I-V Characteristic across Input Ranges



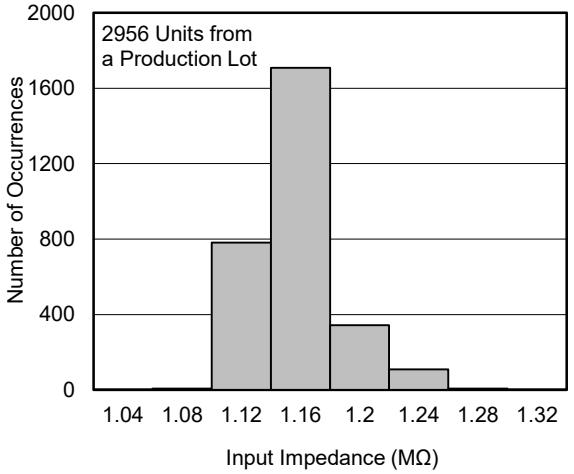
Input I-V Characteristic across Temperature



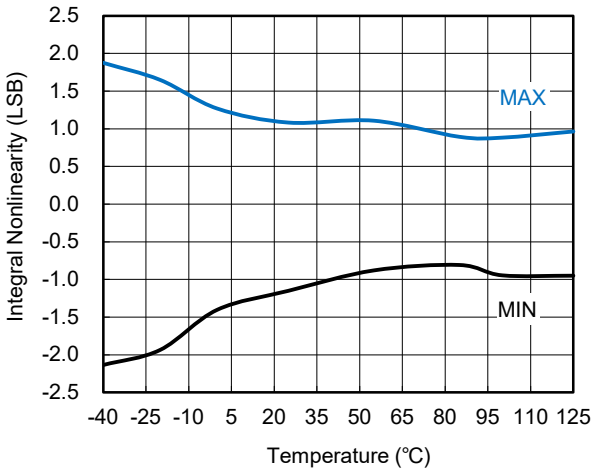
Input Impedance vs. Temperature



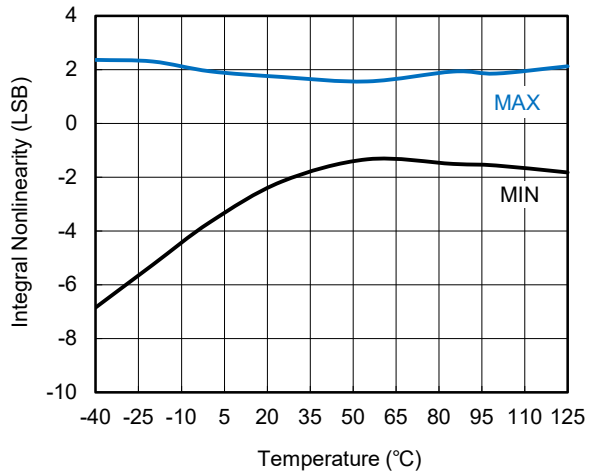
Typical Distribution of Input Impedance



INL vs. Temperature (Bipolar Ranges)

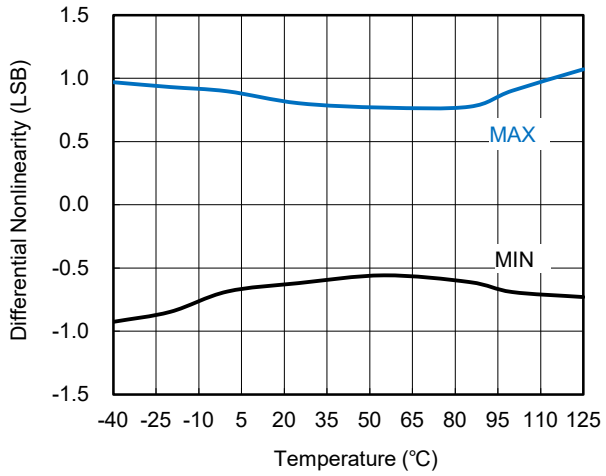


INL vs. Temperature (Unipolar Ranges)

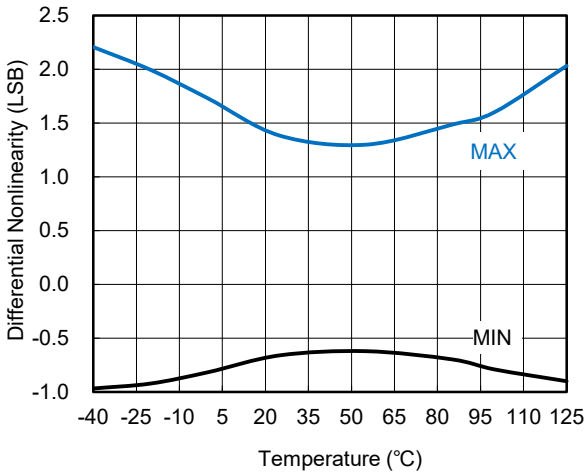


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

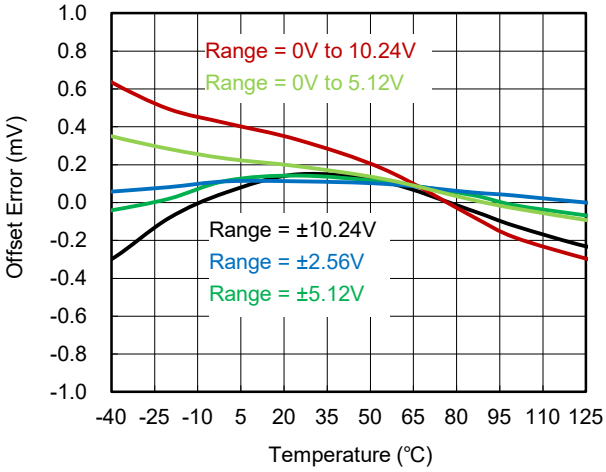
DNL vs. Temperature (Bipolar Ranges)



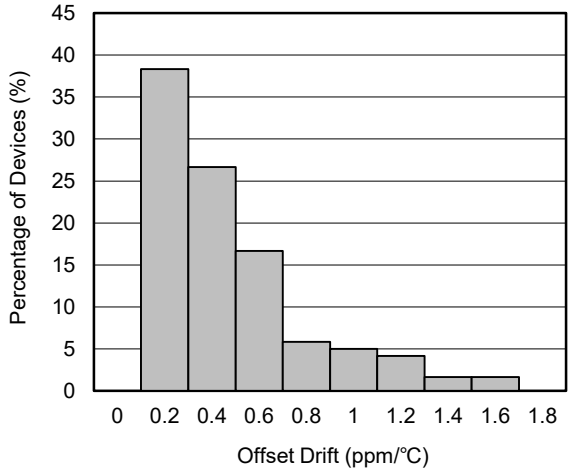
DNL vs. Temperature (Unipolar Ranges)



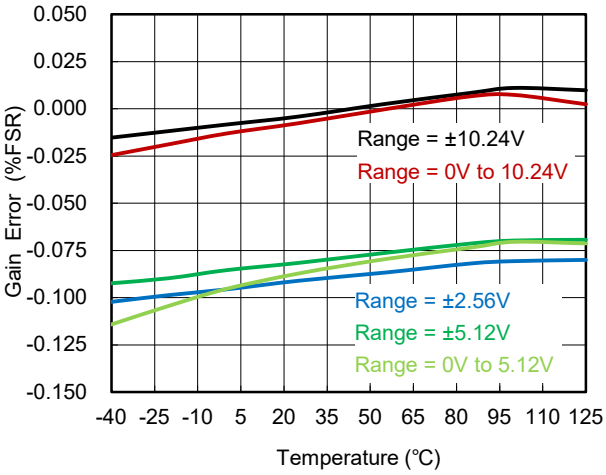
Offset Error vs. Temperature



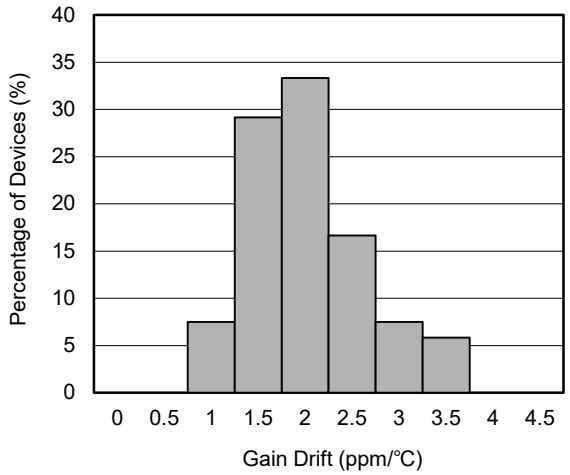
Typical Histogram for Offset Drift



Gain Error vs. Temperature

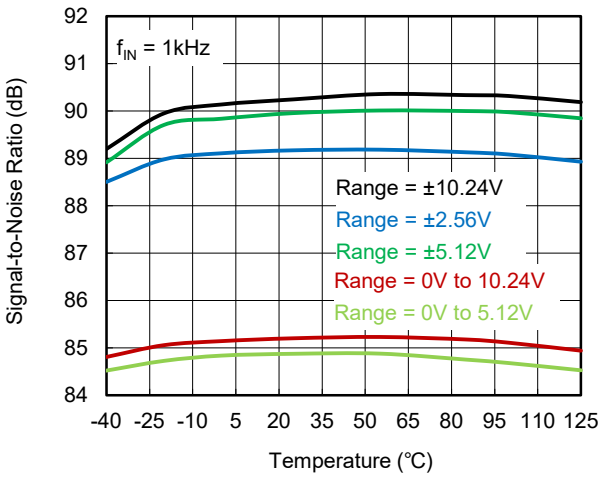


Typical Histogram for Gain Error Drift

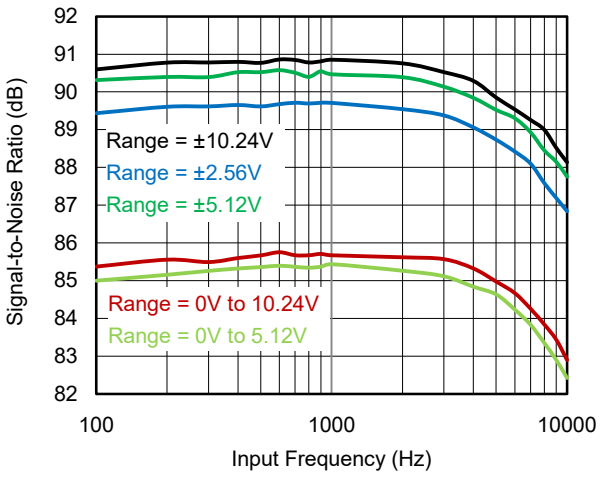


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

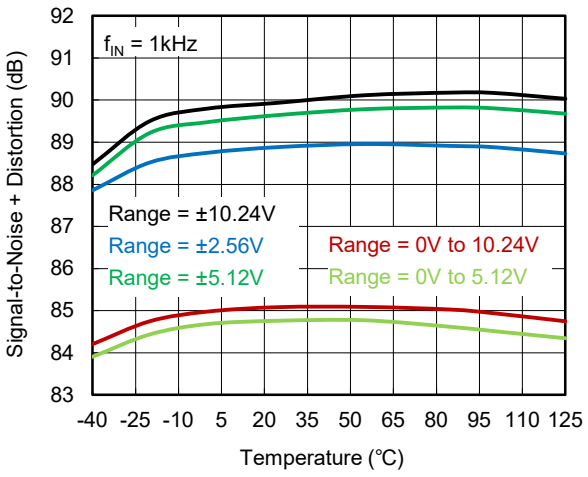
SNR vs. Temperature



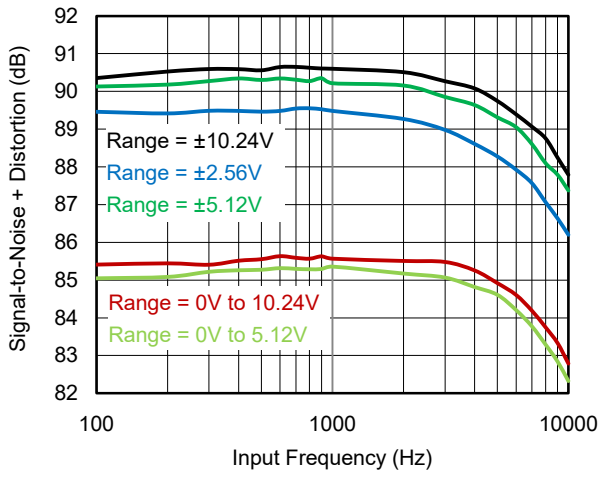
SNR vs. Input Frequency



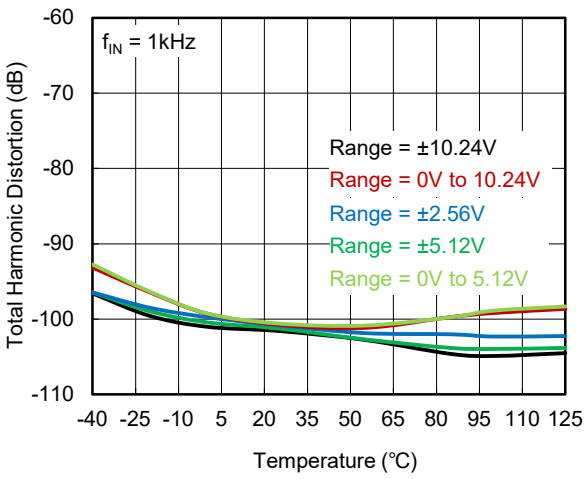
SINAD vs. Temperature



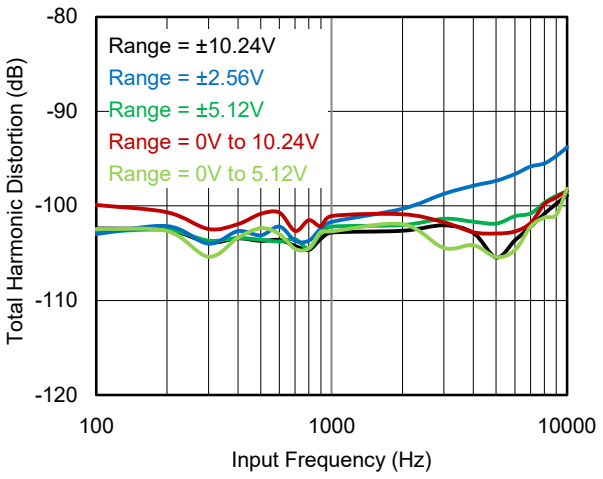
SINAD vs. Input Frequency



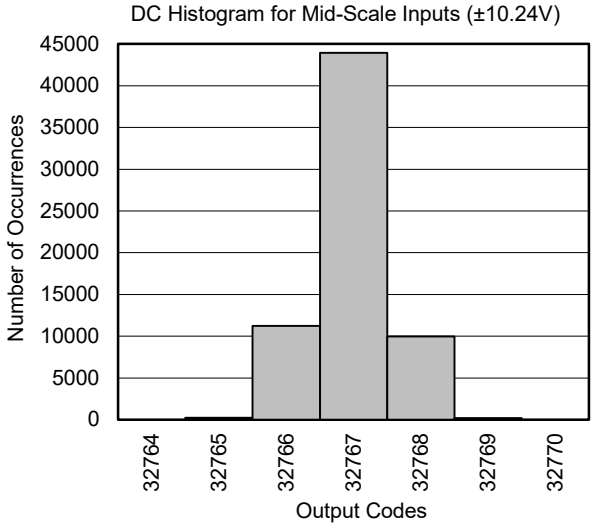
THD vs. Temperature

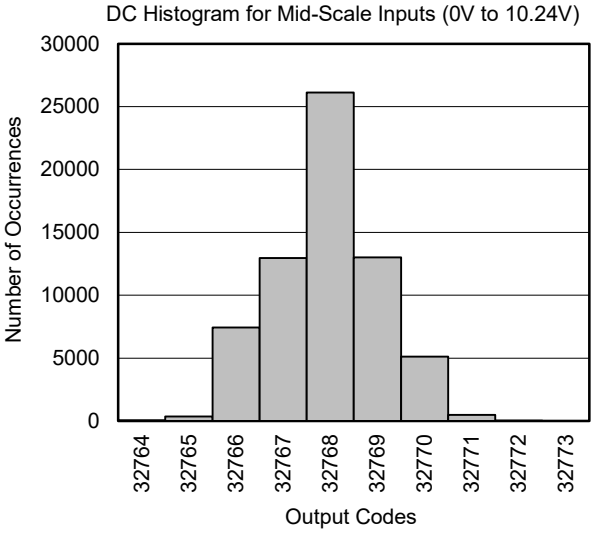


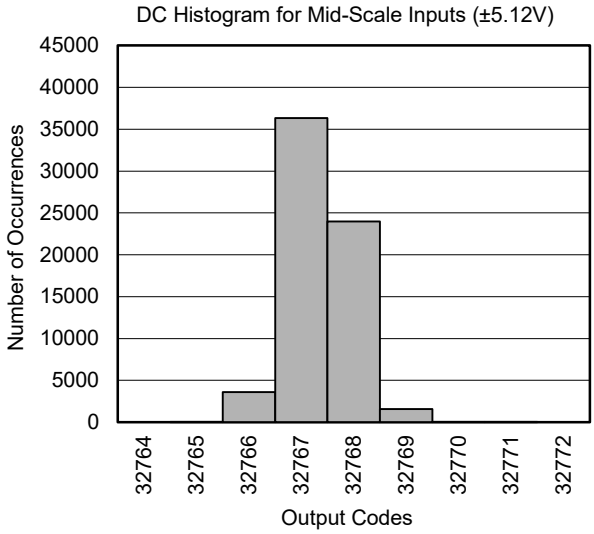
THD vs. Input Frequency

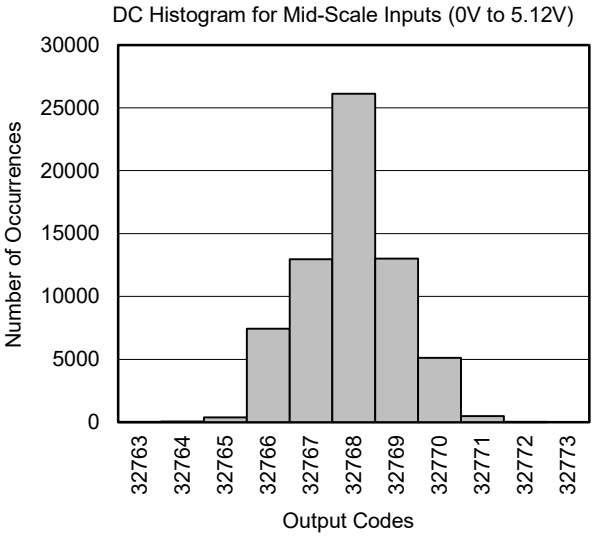


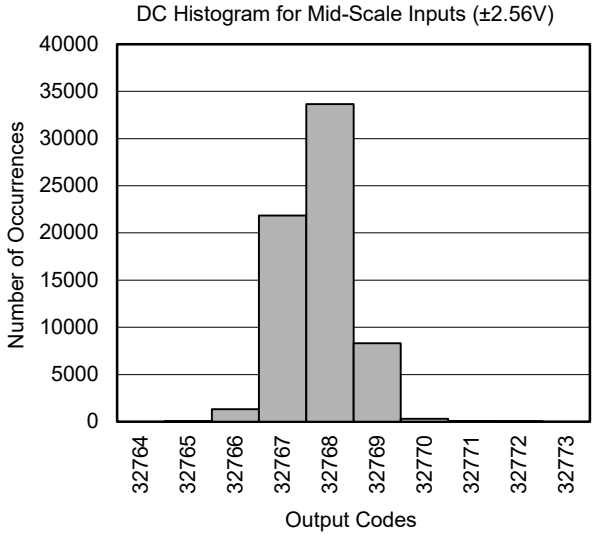
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

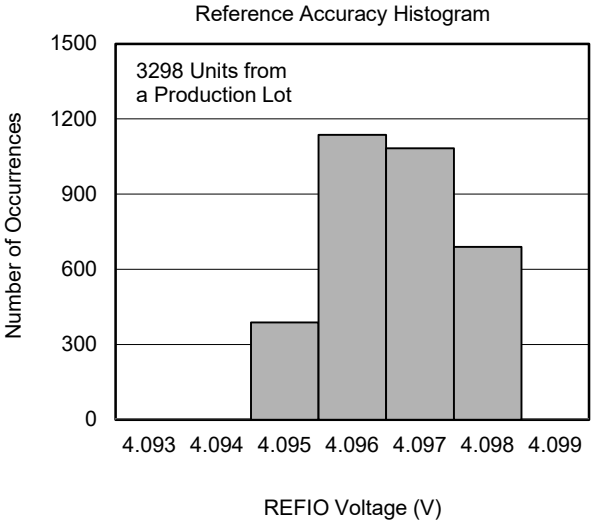






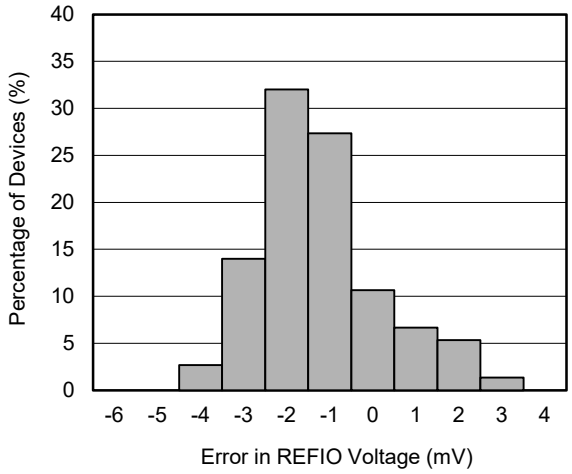




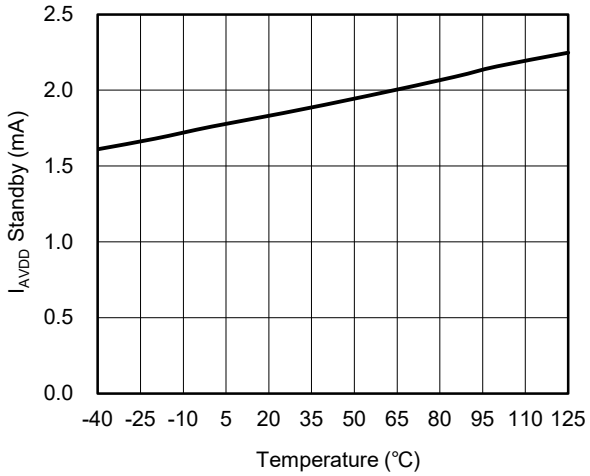


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

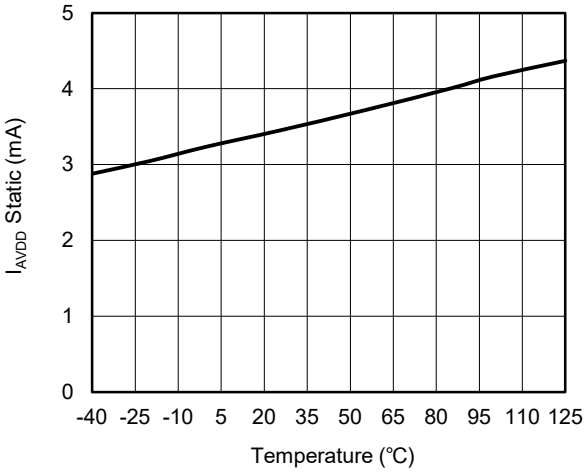
Solder Heat Shift Distribution Histogram



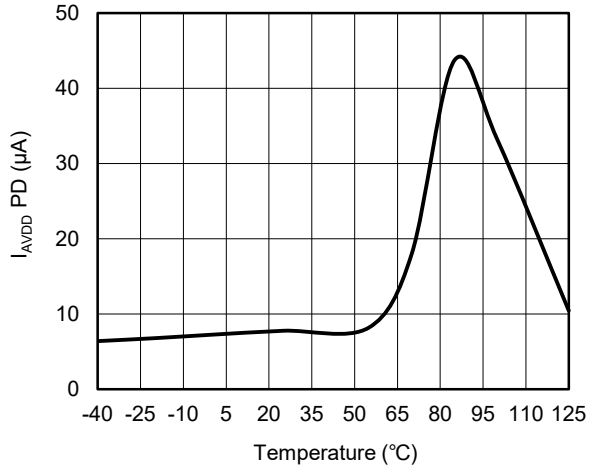
AVDD Current vs. Temperature (Standby Mode)



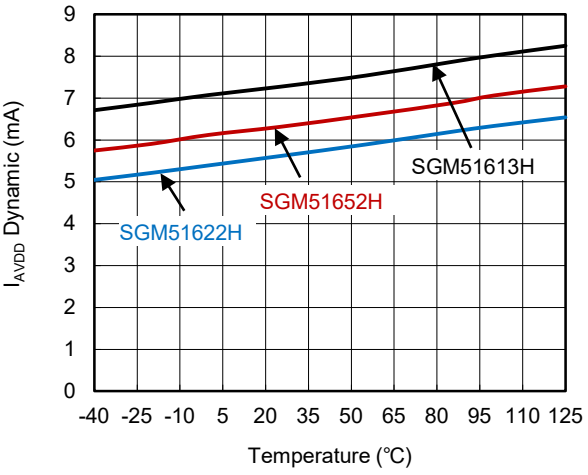
AVDD Current vs. Temperature (During Sampling)



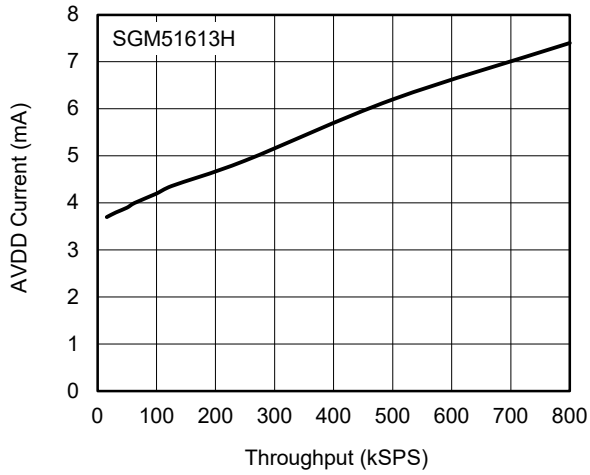
AVDD Current vs. Temperature (Power-Down Mode)



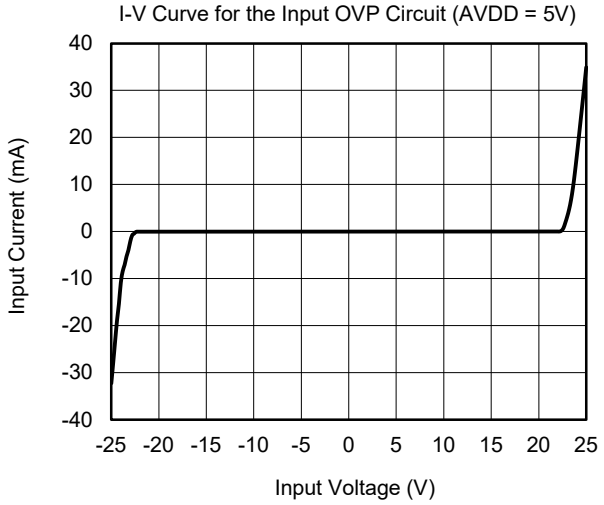
AVDD Current vs. Temperature

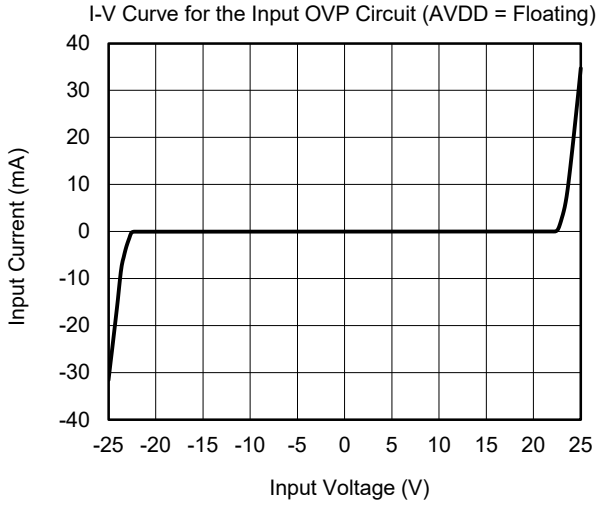


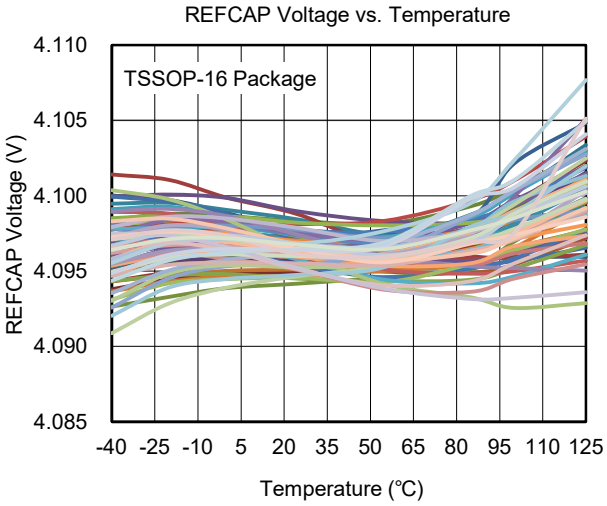
AVDD Current vs. Throughput

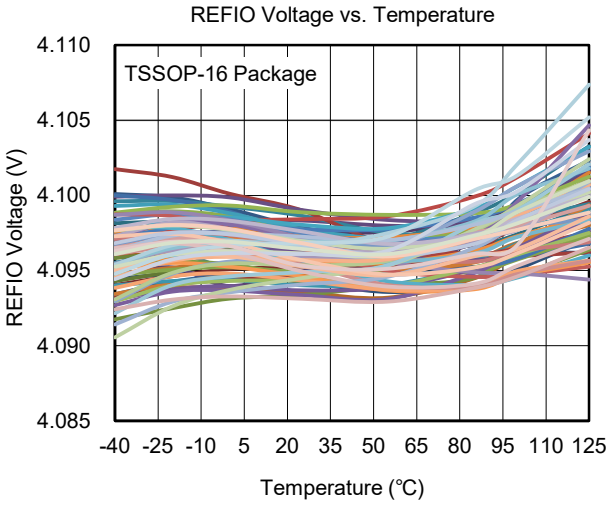


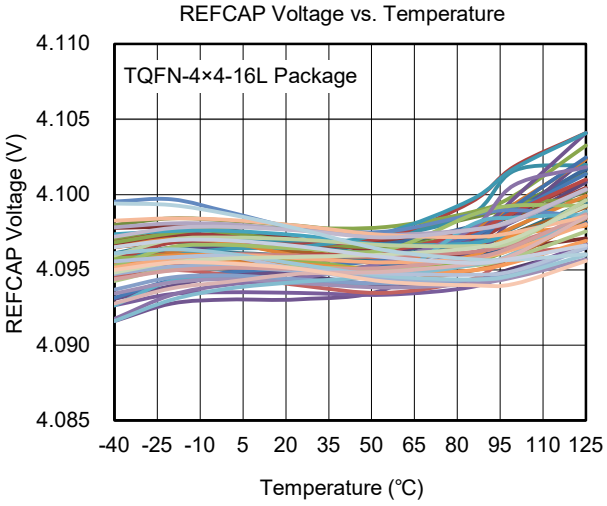
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

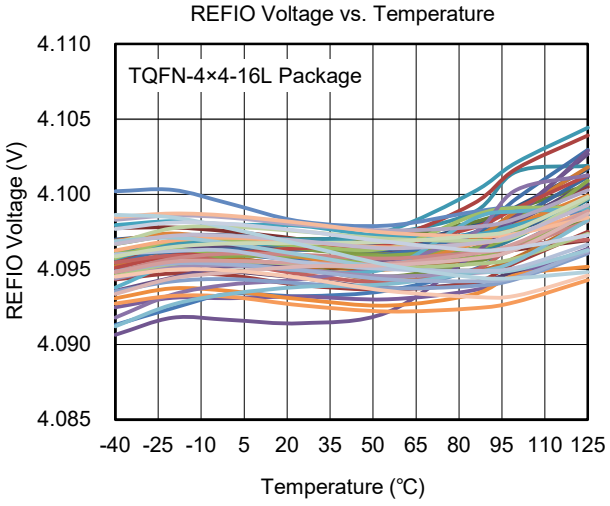






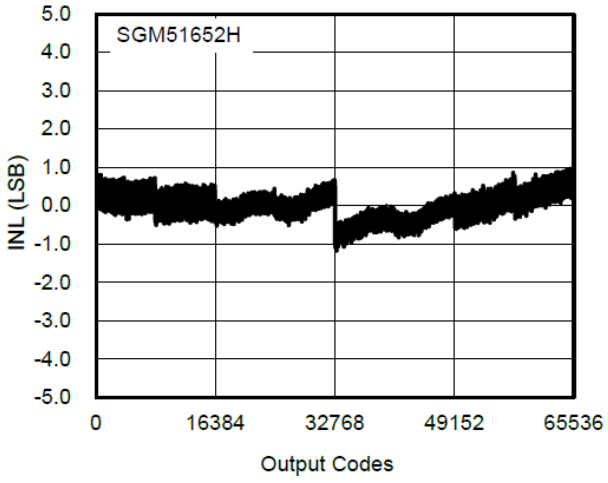




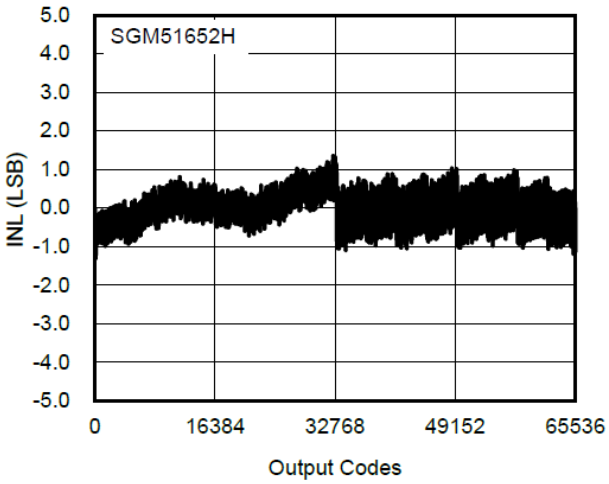


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

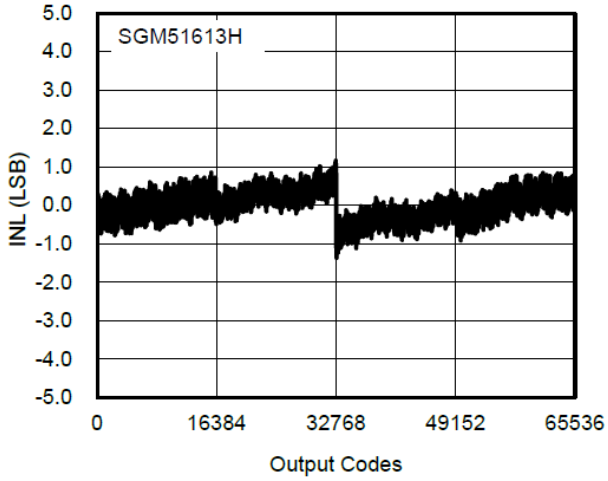
Typical INL for All Codes (Bipolar Ranges)



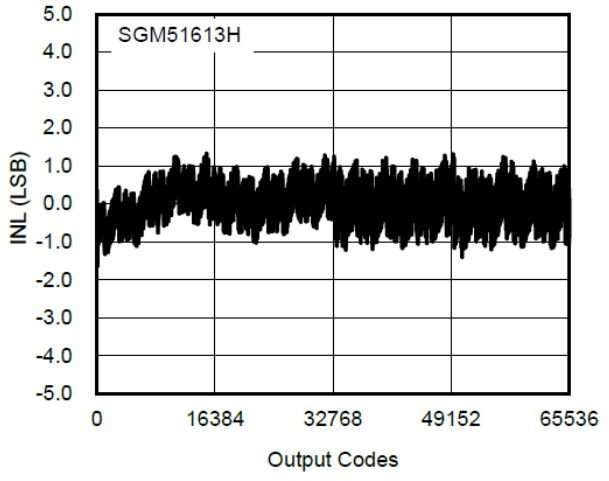
Typical INL for All Codes (Unipolar Ranges)



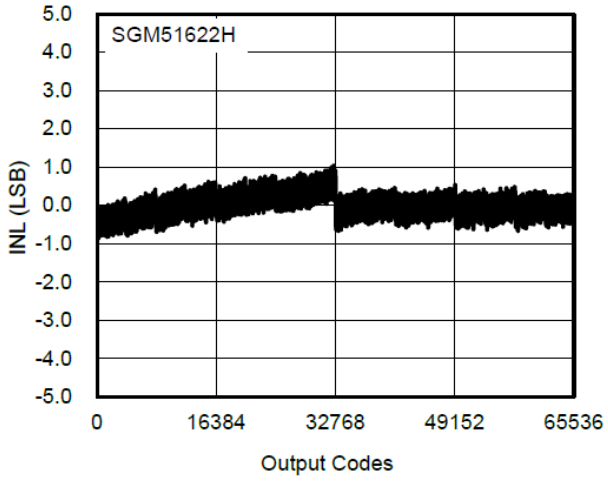
Typical INL for All Codes (Bipolar Ranges)



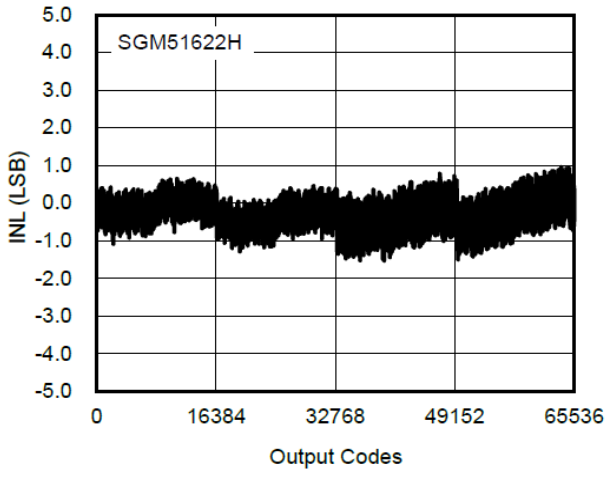
Typical INL for All Codes (Unipolar Ranges)



Typical INL for All Codes (Bipolar Ranges)

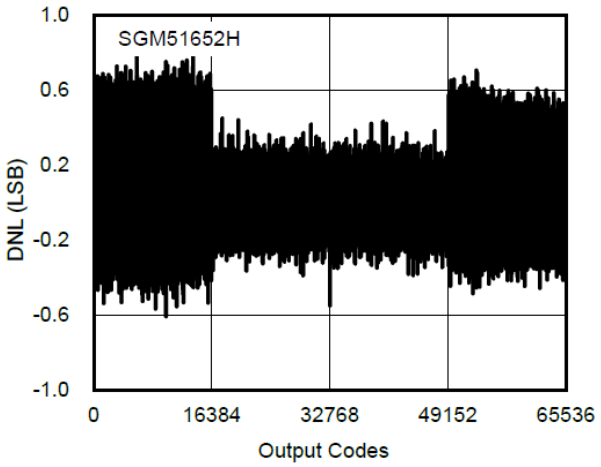


Typical INL for All Codes (Unipolar Ranges)

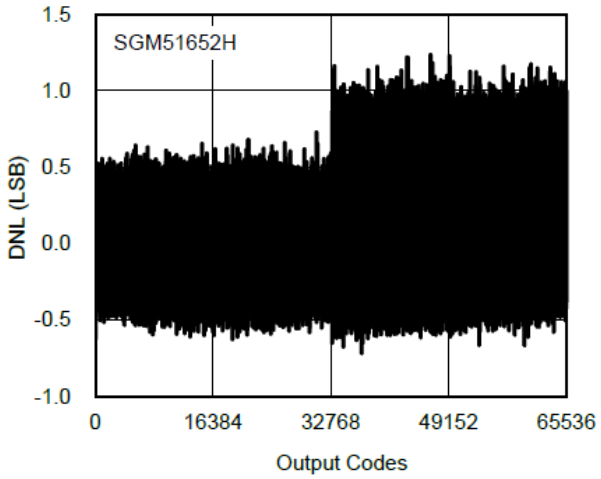


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

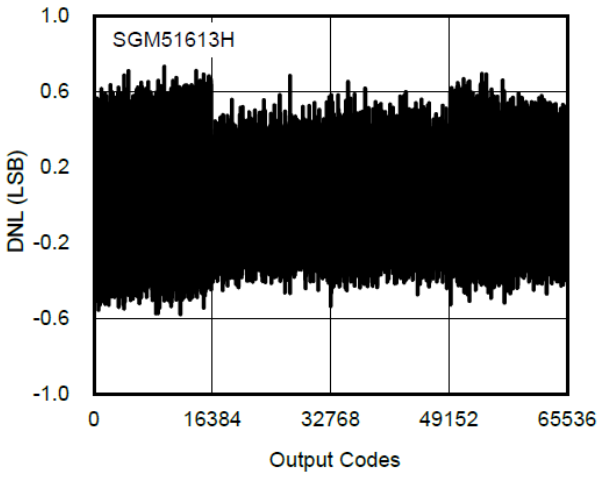
Typical DNL for All Codes (Bipolar Ranges)



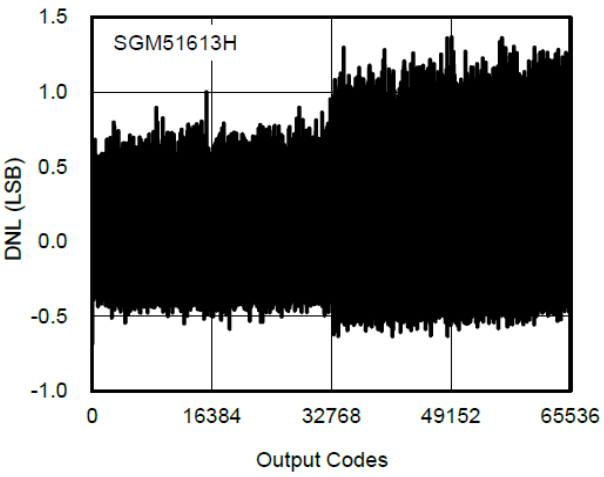
Typical DNL for All Codes (Unipolar Ranges)



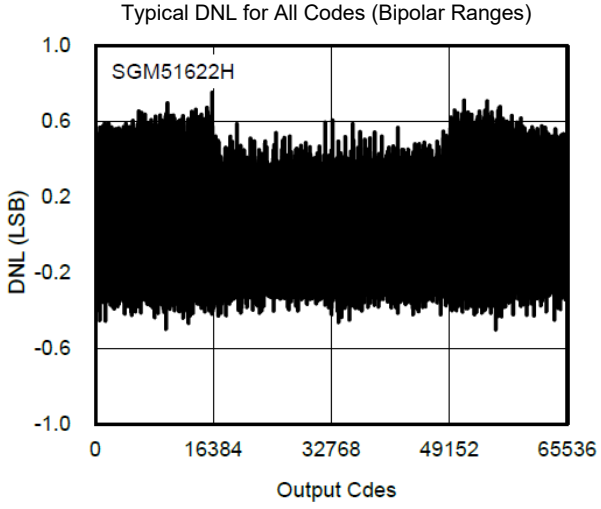
Typical DNL for All Codes (Bipolar Ranges)



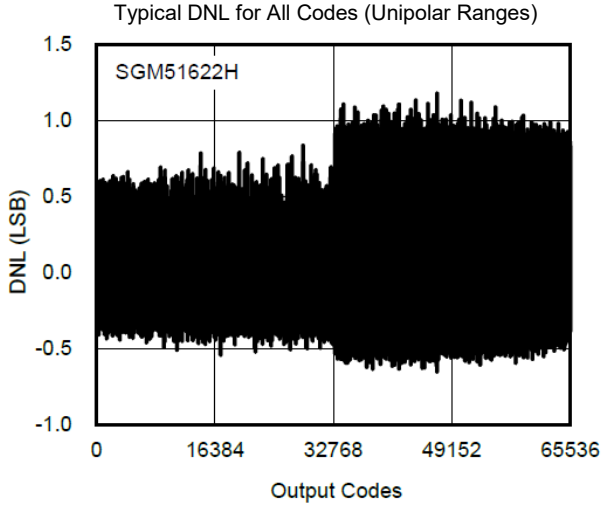
Typical DNL for All Codes (Unipolar Ranges)



Typical DNL for All Codes (Bipolar Ranges)

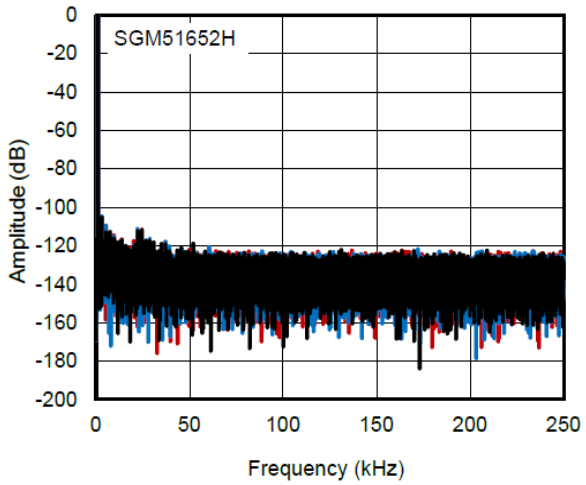


Typical DNL for All Codes (Unipolar Ranges)

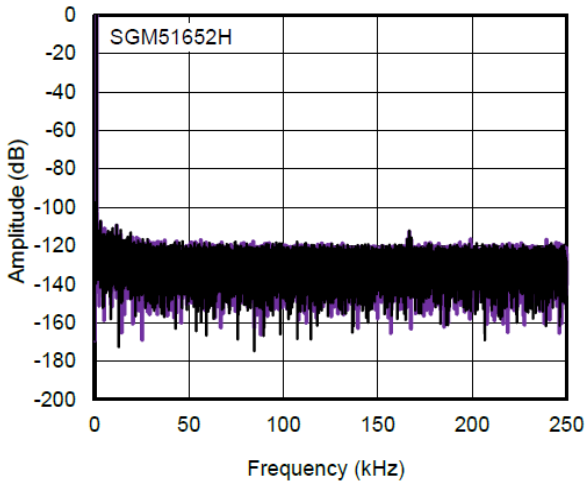


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

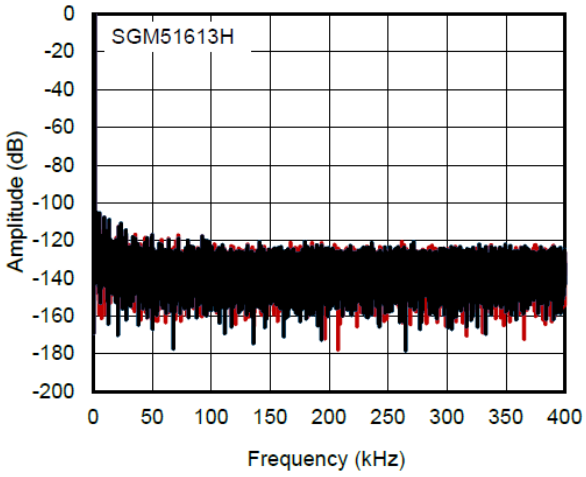
Typical FFT Plot (Bipolar Ranges)



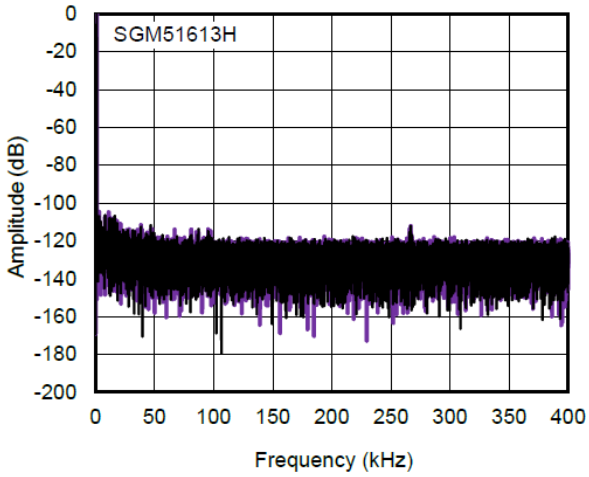
Typical FFT Plot (Unipolar Ranges)



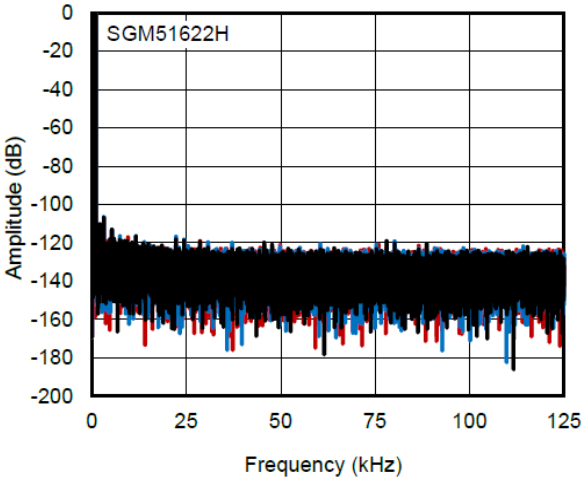
Typical FFT Plot (Bipolar Ranges)



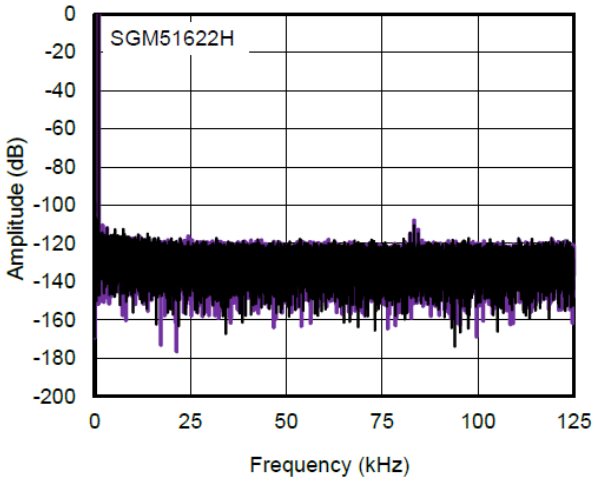
Typical FFT Plot (Unipolar Ranges)



Typical FFT Plot (Bipolar Ranges)



Typical FFT Plot (Unipolar Ranges)



FUNCTIONAL BLOCK DIAGRAM

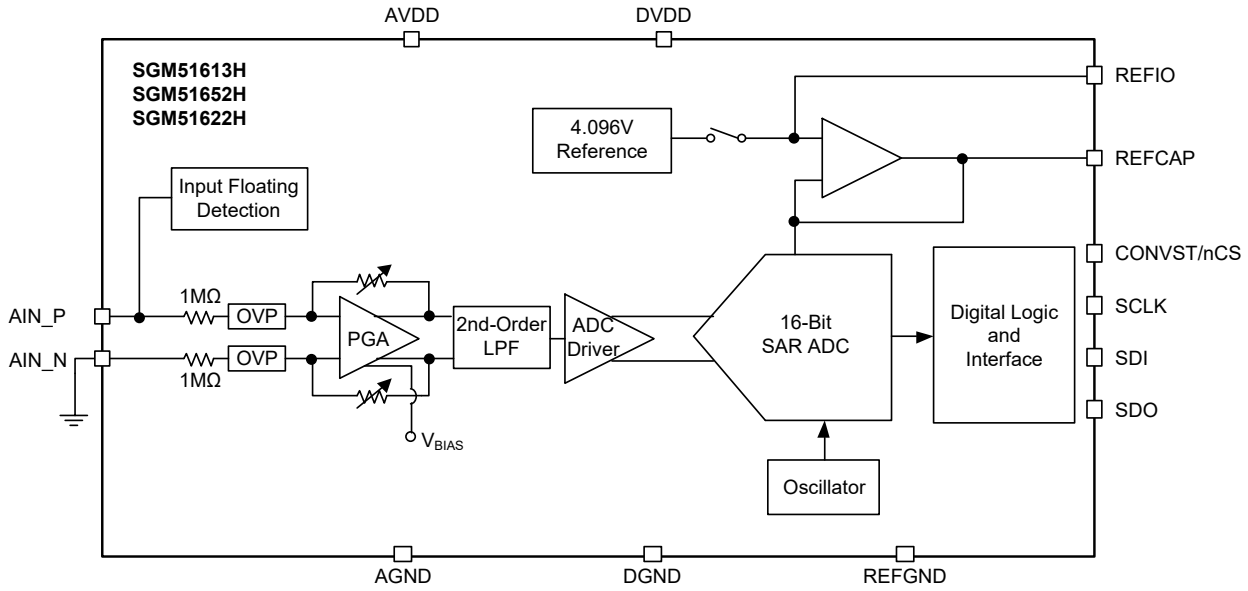


Figure 5. Block Diagram

DETAILED DESCRIPTION

Analog Input Structure

The chip supports bipolar single-ended input, bipolar differential input, and unipolar single-ended input.

When it works in bipolar single-ended input, tie the AIN_N to AGND (system ground), the signal applied to AIN_P can be bipolar ±2.5 × V_{REF}, ±1.25 × V_{REF}, and ±0.625 × V_{REF}. Another selection is that tie the AIN_P to AGNG (system ground), the signal applied to AIN_N can be bipolar ±2.5 × V_{REF}, ±1.25 × V_{REF}, and ±0.625 × V_{REF}.

When it works in unipolar single-ended input, tie the AIN_N to AGND (system ground), the signal applied to AIN_P can be unipolar 0 to 2.5 × V_{REF}, and 0 to 1.25 × V_{REF}.

When it works in bipolar differential input, then AIN_N and AIN_P are differential inputs referring to AGND. For each pin, the absolute voltage referring to AGND must be within the limited voltage specified in electrical characteristic table, at same time, the differential voltage of AIN_P-AIN_N must be compatible with the according input ranges. The common mode voltage of AIN_P and AIN_N are limited in according input ranges. Please refer to electrical characteristic table. When the chip works in bipolar differential input, the valid input ranges are bipolar ±2.5 × V_{REF}, ±1.25 × V_{REF}, and ±0.625 × V_{REF}. The illustrative input signals are shown in Figure 6, as shown in this example, if input common mode voltage is not 0V, there will be some dynamic range (ADC conversion code) losing accordingly.

The input voltage range is configured by software, and it can be bipolar ±2.5 × V_{REF}, ±1.25 × V_{REF}, and ±0.625 × V_{REF} or unipolar 0 to 2.5 × V_{REF}, and 0 to 1.25 × V_{REF}. If there is a reference voltage of 4.096V (internal or external), then the input ranges of the device can be configured to bipolar ranges of ±10.24V, ±5.12V, and ±2.56V or unipolar ranges of 0V to 10.24V, and 0V to 5.12V.

Analog Input Impedance

The input impedance of each channel is ~1MΩ.

Input Over-Voltage Protection Circuit

The chip has the input over-voltage protection (OVP) circuit. Table 1 shows these characteristics.

In the following condition, the input signal is applied before analog AVDD is powered on or the input signal is applied and keep analog AVDD floating, the input OVP circuits will be on. And if the input voltage exceeds the $|V_{OVP}|$, the chip will be damaged.

Input Floating Detection Function

The device features an input floating detection function, when this function is enabled by setting INPUT_FLOATING _DETECTION_EN register corresponding bit. Besides setting the INPUT_FLOATING_DETECTION_EN register, it also needs a pull-down resistor 10MΩ connected to system ground (GND), please refer to typical connection in Figure 7. If perform an input floating detection operating sequences when the input is floating, the corresponding bit in the INPUT_FLOATING_DETECTION_STATUS register is set to '1'. The detailed sequence of operations is shown in Figure 11.

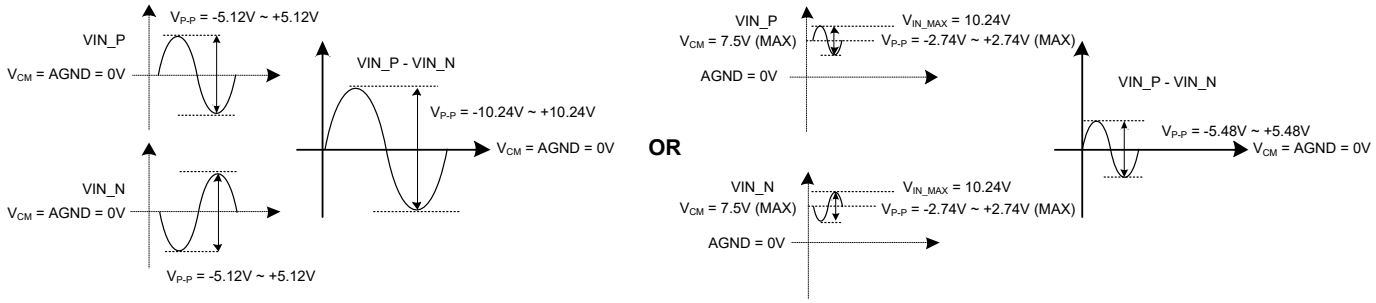
Note that, to perform a complete input floating detection, there must be a consecutive 256 times conversions, which cannot be interrupted by normal input sampling. At same time, if there is still an input signal at input pin, the input floating detection will report an untrusted result.

Table 1. Input Over-Voltage Protection Limits when AVDD = 5V (1)

Input Condition (V_{OVP} = ±20V)	ADC Output	Comments
$\|V_{IN}\| < \|V_{RANGE}\|$	Valid	Work normally.
$\|V_{RANGE}\| < \|V_{IN}\| < \|V_{OVP}\|$	Saturated	ADC output is saturated, and the internal protection circuits are on.
$\|V_{IN}\| > \|V_{OVP}\|$	Saturated	This may damage the chip.

NOTE: 1. AGND = 0V, $|V_{RANGE}|$ is the maximum input voltage for any selected input range, and $|V_{OVP}|$ is the break-down voltage for the internal OVP circuit. Assume that R_S is approximately 0Ω.

DETAILED DESCRIPTION (continued)



NOTE: V_{CM} means common mode voltage. V_{P-P} means peak-to-peak voltage.

Figure 6. Examples of Bipolar Differential ±10.24V Input

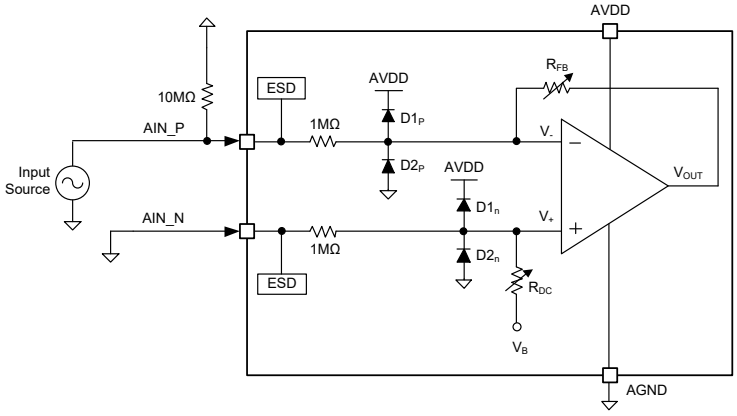


Figure 7. Input Floating Detection Connection

Programmable Gain Amplifier (PGA)

The chip has a programmable gain amplifier (PGA), and the PGA gain can be adjusted by setting the RANGE_SEL[3:0] bits in the configuration register (see the RANGE_ SELECTION register), refer to Table 2.

Table 2. Input Range Selection Bits Details

Analog Input Range	RANGE_SEL[3:0]			
	Bit 3	Bit 2	Bit 1	Bit 0
±2.5 × V_{REF} (default)	0	0	0	1
±1.25 × V_{REF}	0	0	1	1
±0.625 × V_{REF}	0	1	0	0
0 to 2.5 × V_{REF} (1)	1	0	0	1
0 to 1.25 × V_{REF} (1)	1	0	1	1

NOTE: 1. These two unipolar input ranges are only valid for unipolar single-ended input with AIN_N = AGND.

Second-Order, Low-Pass Filter (LPF)

The chip has a second-order, antialiasing LPF at the output of the PGA.

Reference

The chip can be operated with an internal reference or an external voltage reference.

ADC Description

The chip output code is in straight-binary format.

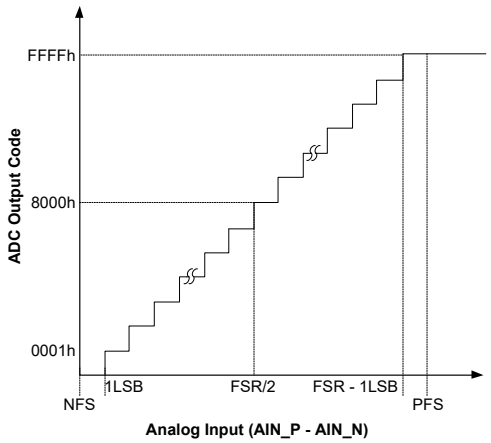


Figure 8. Device Transfer Function (Straight-Binary Format)

DETAILED DESCRIPTION (continued)

Table 3. ADC LSB Values for Different Input Ranges (V_{REF} = 4.096V)

Input Range	Positive Full-Scale (V)	Negative Full-Scale (V)	Full-Scale Range (V)	LSB (μV)
±2.5 × V_{REF}	10.24	-10.24	20.48	312.5
±1.25 × V_{REF}	5.12	-5.12	10.24	156.25
±0.625 × V_{REF}	2.56	-2.56	5.12	78.125
0 to 2.5 × V_{REF} (1)	10.24	0	10.24	156.25
0 to 1.25 × V_{REF} (1)	5.12	0	5.12	78.125

NOTE: 1. These two unipolar input ranges are only valid for unipolar single-ended input with AIN_N = AGND.

Alarm Features

The chip has an active-high alarm output function on the ALARM/SDO-1/GPO pin if the pin is used for ALARM output.

There are two types of alarms: the input alarm and the AVDD alarm.

When each conversion ends, the ALARM output flags are updated internally. The ALARM output flags can be read out in 3 kinds of way. Firstly it can be read by the ALARM output pin, secondly read the internal ALARM registers, thirdly append the ALARM flags to the data output.

Input Alarm

The chip has input low and input high alarm. These alarms have a common hysteresis window which can be set by ALARM_HIGH_THRES and ALARM_LOW_THRES registers.

Please see the trigged function diagrams in Figure 9 and Figure 10.

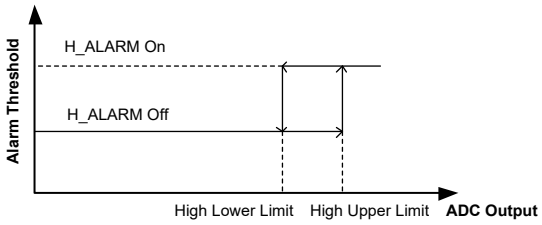


Figure 9. High ALARM Hysteresis

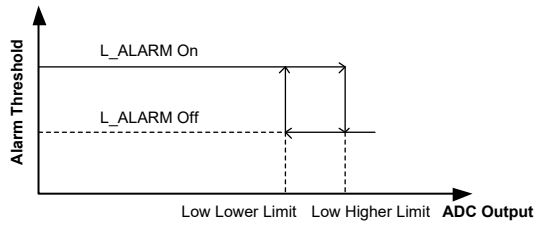


Figure 10. Low ALARM Hysteresis

AVDD Alarm

If the AVDD exceeds 5.35V (TYP) or drops below 4.62V (TYP), there is an AVDD alarm.

SPI Connection Topologies

Single Device: Standard SPI Interface

The chip supports a standard SPI protocol and connection.

Multiple Devices: Daisy-Chain Topology

The chip supports the daisy-chain connection.

Device Operational Modes

The chip supports three functional states: RESET, Acquisition, and Conversion. The state is determined by the status of the CONVST/nCS and RST control signals.

RESET State

To issue a RESET, the nRST pin must be pulled low and kept low for a specified time (see Timing Characteristics in Figure 2). The chip has two different reset functions: an application reset and a power-on reset (POR). The function of the nRST pin is determined by the state of the RSTn_APP bit in the RESET_POWER_CONTROL register.

To issue an application reset, the RSTn_APP bit must be set to 1. In this RESET status, according configuration registers are reset to the default values (please refer to registers descriptions, note that an application reset is not as same as power-on reset), the RADC_ADCS pin keeps low, and the SDO-x pins are tri-stated.

To issue a power-on reset, the RSTn_APP bit is set to 0. In POR status, all internal circuits of the chip (including the PGA, ADC driver, and voltage reference) are reset.

To exit the RESET status, pull the nRST pin high while keep the CONVST/nCS and SCLK pins low.

Acquisition State

The chip enters acquisition state after system powers up, or after reset, or at the end of every conversion.

Conversion State

On the rising edge of CONVST/nCS signal, the chip transits from acquisition state to conversion state. The conversion process is driven by the internal clock. During the conversion, the chip is not response to CONVST/nCS signal. See the timing table, under the different sampling speed, the minimum sampling time and conversion time must be met.

DETAILED DESCRIPTION (continued)

Digital Interface Operation (SPI Interface Operation)

Data Transfer Frame

For a typical data transfer frame, the controller pulls CONVST/nCS low to initiate the data transfer frame.

At the end of the data transfer frame:

• If the SCLK counter = 32, the chip treats the frame as a valid operation.

• If the SCLK counter is < 32, the chip treats the frame as an invalid operation. In a write operation, the command is ignored. In a read operation, the according number of MSB bits is shifted from 32-bit register.

• If the SCLK counter is > 32, the chip treats the frame as a long frame operation. The last 32 bits is accepted before the CONVST/nCS rising edge.

Input Command Word and Register Write Operation

The chip supports one byte or two bytes (equivalent to half a word) operation. Table 4 lists the input commands. In a single operation, the command composed of two types is marked by HWORD (Half of a WORD).

In an HWORD command, the LSB bit of 9-bit address is treated as 0. For example, whether the address is 0b000010000 or 0b000010001, the chip executes the command with the address 0b000010000.

Table 4. Input Commands List

OPCODE Bit [31:0]	Command	Description
00000000_000000000_ 00000000_00000000	NOP	No operation.
11000_xx_<9-bit address>_ <16-bit data> (1)	CLEAR_HWORD	Clear Any Bits of a Register 16-bit data, DB[15:0], DB[x] = 1, means that clear the specified bit to '0' in the address register. DB[x] = 0, means unchanged.
11001_xx_<9-bit address>_ 00000000_00000000	READ_HWORD	Issue a 16-Bit Read Operation Followed this command, the chip shifts out 16-bit of the register content in the next frame.
01001_xx_<9-bit address>_ 00000000_00000000	READ	Same as the READ_HWORD, only 8-bit of the register content is returned in the next frame.
11010_00_<9-bit address>_ <16-bit data>	WRITE	Half-Word Write Command 16-bit data, DB[15:0] is written to the addressed register.
11010_01_<9-bit address>_ <16-bit data>		High-Byte Write Command 16-bit data, DB[15:0], only DB[15:8] is written to the addressed register. DB[7:0] is ignored.
11010_10_<9-bit address>_ <16-bit data>		Low-Byte Write Command 16-bit data, DB[15:0], only DB[7:0] is written to the addressed register. DB[15:8] is ignored.
11011_xx_<9-bit address>_ <16-bit data>	SET_HWORD	Set Any Bits of a Register 16-bit data, DB[15:0], DB[x] = 1, means that set the specified bit to '1' in the address register. DB[x] = 0, means unchanged.
All other input command combinations	NOP	No operation.

NOTE:
1. <9-bit address> is composed of MSB '0' and an 8-bit register address (which is shown in Table 8). For example, the <9-bit address> for register 0x08 is 0b000001000.

DETAILED DESCRIPTION (continued)

Output Data Word

In any operation, the 32-bit content of frame N+1 is determined by the command in frame N and the set of DATA_VAL[2:0] bits (which is in the DATAOUT_CONTROL register). If DATA_VAL[2:0] is set to 1xx, the data format is described in the DATAOUT_CONTROL register. If a READ command is in frame N, the output of frame N+1 is 8-bit register data and others followed by '0'. If a READ_HWORD command is in frame N, the output of frame N+1 is 16-bit register data and others followed by '0'.

For the other combinations, the frame N+1 is composed of 16-bit ADC conversion result and various of data flag (depends on the setting of the DATAOUT_CONTROL register). If all flags are enabled, they are in the following sequence: DEVICE_ADDR, AVDD ALARM FLAGS, INPUT ALARM FLAGS, ADC INPUT RANGE FLAGS, PARITY, and all remaining bits are set to 0, see Table 5 for an example. If only some flags are enabled, an example is shown in Table 6.

Table 5. Output Data Word (All Data Flags Enabled) (1)

DB[31:16]	DB[15:12]	DB[11:10]	DB[9:7]	DB[7:4]	DB[3:2]	DB[1:0]
Conversion result	Device address	AVDD alarm flags	Input alarm flags	ADC input range	Parity bits	00

NOTE:
1. DEVICE_ADDR_INCL = 1, VDD_ACTIVE_ALARM_INCL = 1, IN_ACTIVE_ALARM_INCL = 1, RANGE_INCL = 1, and PAR_EN = 1.

Table 6. Output Data Word (Only Some Data Flags Enabled) (1)

DB[31:16]	DB[15:14]	DB[13:10]	DB[9:8]	DB[7:0]
Conversion result	AVDD alarm flags	ADC input range	Parity bits	00000000

NOTE:
1. DEVICE_ADDR_INCL = 0, VDD_ACTIVE_ALARM_INCL = 1, IN_ACTIVE_ALARM_INCL = 0, RANGE_INCL = 1, and PAR_EN = 1.

Input Floating Detection Function Operating Sequences

The device provides a function to detect input floating. To perform this function, it is necessary to follow the operations as bellows. Firstly, enable the control bit in the INPUT_FLOATING_DETECTION_EN register (see Table 18). Secondly, perform 256 times of conversion. The control bit in the INPUT_FLOATING_DETECTION_EN register will reset automatically after ADC converts 256 times. In the process of 256 conversions, if there is no input floating default, all conversion data are normal conversion results which can be used for user. Thirdly, read the status bit in the INPUT_FLOATING_DETECTION_STATUS register (see Table 19). Note that the alarm bit in the INPUT_FLOATING_DETECTION_STATUS register will not be cleared, until an input floating detection operation is performed again and the input of ADC is connected to an input signal source. For an example operation sequences, please refer to Figure 11.

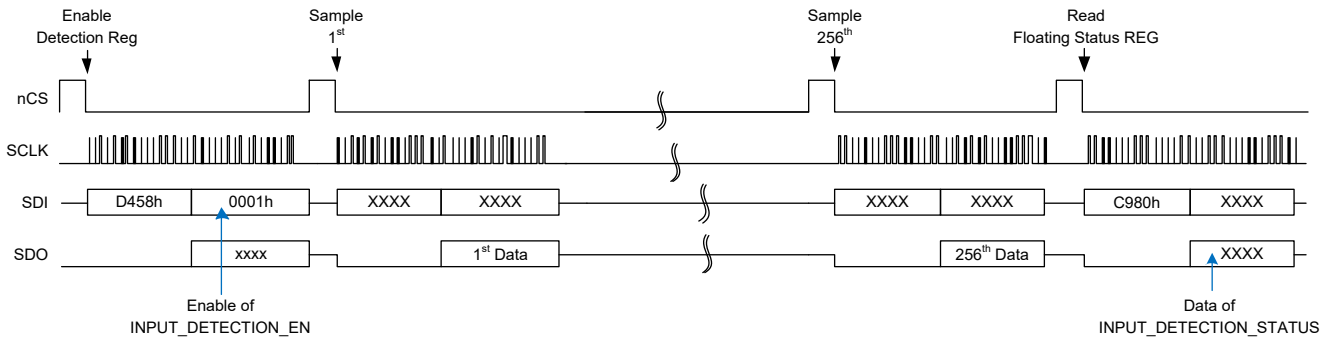


Figure 11. Input Floating Detection Operating Sequences

DETAILED DESCRIPTION (continued)

SPI Protocols

Protocols for Configuring the Device

The chip supports all 4 types of SPI protocols. After system power-on or reset, the default mode is SPI-00-S (CPHA = 0 and CPOL = 0).

Protocols for Reading from the Device

The data read operation protocols are roughly divided into two types: one is SPI-compatible protocols with a single SDO-x, and the other is SPI-compatible protocols with dual SDO-x.

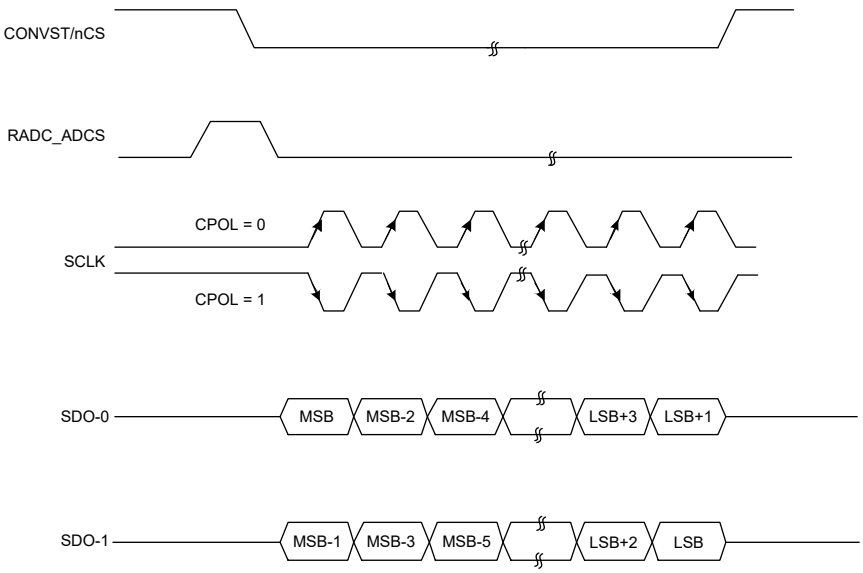
SPI-Compatible Protocols with a Single SDO-x

As shown in Table 7, the chip supports all 4 types of SPI protocols. After system power-on or reset, the default mode is SPI-00-S (CPHA = 0 and CPOL = 0).

Table 7. SPI Protocols for Reading from the Device

Protocol	SCLK Polarity (At nCS Falling Edge)	SCLK Phase (Capture Edge)	MSB Bit Launch Edge	SDI_CONTROL	SDO_CONTROL
SPI-00-S	Low	Rising	nCS falling	00h	00h
SPI-01-S	Low	Falling	1st SCLK rising	01h	00h
SPI-10-S	High	Falling	nCS falling	02h	00h
SPI-11-S	High	Rising	1st SCLK falling	03h	00h

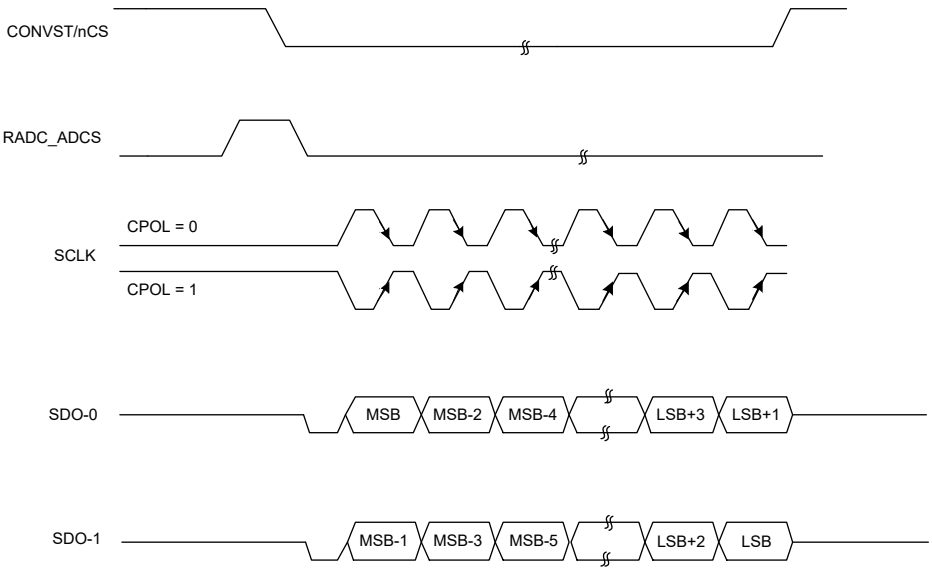
SPI-Compatible Protocols with Dual SDO-x



NOTE: In dual SDO modes, the amount of SCLK required by the chip is only half that in single SDO modes.

Figure 12. Standard SPI Timing Protocol (CPHA = 0, Dual SDO-x)

DETAILED DESCRIPTION (continued)



NOTE: In dual SDO modes, the amount of SCLK required by the chip is only half that in single SDO modes.

Figure 13. Standard SPI Timing Protocol (CPHA = 1, Dual SDO-x)

REGISTER MAPS

Bit Types:
R/W: Read/Write bit(s)
R: Read only bit(s)

Device Configuration and Register Maps

The device has 11 configuration registers, the register maps are shown in Table 8. Each configuration register consists of four data bytes, which can be reached by their unique address.

Table 8. Configuration Register Maps

Address	Register Name	Register Function
00h	CHIP_ID	CHIP_ID Register
04h	RESET_POWER_CONTROL	Reset and Power Control Register
08h	SDI_CONTROL	SDI Data Input Control Register
0Ch	SDO_CONTROL	SDO-x Data Input Control Register
10h	DATAOUT_CONTROL	Output Data Control Register
14h	RANGE_SELECTION	Input Range Selection Control Register
20h	ALARM_OUTPUT	ALARM Output Register
24h	ALARM_HIGH_THRES	ALARM High Threshold and Hysteresis Register
28h	ALARM_LOW_THRES	ALARM Low Threshold Register
2Ch	INPUT_FLOATING_DETECTION_EN	Input Floating Detection Enable Register
30h	INPUT_FLOATING_DETECTION_STATUS	Input Floating Detection Status Register

CHIP_ID Register (Address = 00h)

This register can be set a unique identification address associated to a device that is used in a daisy-chain system.

Table 9. CHIP_ID Register Details

BITS	BIT NAME	POWER-ON RESET (2)	APPLICATION RESET (3)	TYPE	DESCRIPTION
D[31:24]	Reserved	00h	00h	R	Reserved.
D[23:20]	Reserved	0000b	0000b	R	Reserved.
D[19:16]	DEVICE_ADDR[3:0]	0000b	0000b	R/W	These bits can be used to address different devices in the system. The amount of the devices can be up to 16. These bits are useful in daisy-chain mode.
D[15:0]	Reserved	0000h	0000h	R	Reserved.

NOTES:
1. Address for bits [7:0] = 00h. Address for bits [15:8] = 01h. Address for bits [23:16] = 02h. Address for bits [31:24] = 03h.
2. Power-on reset valid.
3. Application reset valid.

REGISTER MAPS (continued)

RESET_POWER_CONTROL Register (Address = 04h)

Table 10. RESET_POWER_CONTROL Register Details

BITS	BIT NAME	POWER-ON RESET (2)	APPLICATION RESET (3)	TYPE	DESCRIPTION
D[31:16]	Reserved	0000h	0000h	R	Reserved.
D[15:8]	WKEY[7:0]	00h	00h	R/W	A Key Function. Any writing to D[5:0] operation is accepted on condition that the WKEY[7:0] is set to 69h first.
D[7:6]	Reserved	00b	00b	R	Reserved.
D[5]	VDD_AL_DIS	0b	0b	R/W	0 = VDD alarm is enabled (default) 1 = VDD alarm is disabled
D[4]	IN_AL_DIS	0b	0b	R/W	0 = Input alarm is enabled (default) 1 = Input alarm is disabled
D[3]	Reserved	0b	0b	R	Reserved.
D[2]	RSTn_APP	0b	–	R/W	0 = nRST pin functions as a POR class reset (causes full device initialization) (default) 1 = nRST pin functions as an application reset (only user-programmed modes are cleared) The setting will be power-on reset to default.
D[1]	NAP_EN	0b	–	R/W	0 = Disable the NAP mode (default) 1 = Enable the NAP mode Details on the latency encountered when entering and exiting the relevant low-power mode, see Electrical Characteristics section.
D[0]	PWRDN	0b	0b	R/W	0 = Disable the power-down mode (default) 1 = Enter the power-down mode Details on the latency encountered when entering and exiting the relevant low-power mode, see Electrical Characteristics section.

NOTES:
1. Address for bits [7:0] = 04h. Address for bits [15:8] = 05h. Address for bits [23:16] = 06h. Address for bits [31:24] = 07h.
2. Power-on reset valid.
3. Application reset valid.

SDI_CONTROL Register (Address = 08h)

Table 11. SDI_CONTROL Register Details

BITS	BIT NAME	POWER-ON RESET (2)	APPLICATION RESET (3)	TYPE	DESCRIPTION
D[31:16]	Reserved	0000h	0000h	R	Reserved.
D[15:8]	Reserved	00h	00h	R	Reserved.
D[7:2]	Reserved	000000b	000000b	R	Reserved.
D[1:0]	SDI_MODE[1:0]	00b	–	R/W	00 = Standard SPI with CPOL = 0 and CPHASE = 0 (default) 01 = Standard SPI with CPOL = 0 and CPHASE = 1 10 = Standard SPI with CPOL = 1 and CPHASE = 0 11 = Standard SPI with CPOL = 1 and CPHASE = 1 These bits set the SPI protocol.

NOTES:
1. Address for bits [7:0] = 08h Address for bits [15:8] = 09h Address for bits [23:16] = 0Ah Address for bits [31:24] = 0Bh.
2. Power-on reset valid.
3. Application reset valid.

REGISTER MAPS (continued)

SDO_CONTROL Register (Address = 0Ch)

Table 12. SDO_CONTROL Register Details

BITS	BIT NAME	POWER-ON RESET (2)	APPLICATION RESET (3)	TYPE	DESCRIPTION
D[31:16]	Reserved	0000h	0000h	R	Reserved.
D[15:13]	Reserved	000b	000b	R	Reserved.
D[12]	GPO_VAL	0b	0b	R/W	1-bit data for the output on the GPO pin.
D[11:10]	Reserved	00b	00b	R	Reserved.
D[9:8]	SDO1_CONFIG[1:0]	00b	00b	R/W	00 = SDO-1 is tri-stated (default) 01 = SDO-1 set as ALARM 10 = SDO-1 set as GPO 11 = SDO-1 work with SDO-0 in 2-bit SDO mode
D[7]	Reserved	0b	0b	R	Reserved.
D[6]	SSYNC_CLK	0b	–	R/W	0 = External SCLK (default) 1 = Internal clock This bit takes effect only in the ADC master clock or source-synchronous mode of operation.
D[5:2]	Reserved	0000b	0000b	R	Reserved.
D[1:0]	SDO_MODE[1:0]	00b	–	R/W	00 and 01 = SDO mode follows the same SPI protocol as that used for SDI. See the SDI_CONTROL register 10 = Invalid configuration 11 = Invalid configuration

NOTES:
1. Address for bits [7:0] = 0Ch. Address for bits [15:8] = 0Dh. Address for bits [23:16] = 0Eh. Address for bits [31:24] = 0Fh.
2. Power-on reset valid.
3. Application reset valid.

REGISTER MAPS (continued)

DATAOUT_CONTROL Register (Address = 10h)

This register controls the data output by the device.

Table 13. DATAOUT_CONTROL Register Details

BITS	BIT NAME	POWER-ON RESET (2)	APPLICATION RESET (3)	TYPE	DESCRIPTION
D[31:16]	Reserved	0000h	0000h	R	Reserved.
D[15]	Reserved	0b	0b	R	Reserved.
D[14]	DEVICE_ADDR_INCL	0b	0b	R/W	0 = Disable SDO-x output including DEVICE_ADDR (default) 1 = Enable SDO-x output including DEVICE_ADDR Select whether DEVICE_ADDR register value in the SDO-x output bit stream.
D[13:12]	VDD_ACTIVE_ ALARM_INCL[1:0]	00b	00b	R/W	00 = Do not include (default) 01 = Include ACTIVE_VDD_H_FLAG 10 = Include ACTIVE_VDD_L_FLAG 11 = Include both flags Select whether VDD ALARM flags in the SDO-x output bit stream.
D[11:10]	IN_ACTIVE_ ALARM_INCL[1:0]	00b	00b	R/W	00 = Do not include (default) 01 = Include ACTIVE_IN_H_FLAG 10 = Include ACTIVE_IN_L_FLAG 11 = Include both flags Select whether input ALARM flags in the SDO-x output bit stream.
D[9]	Reserved	0b	0b	R	Reserved.
D[8]	RANGE_INCL	0b	0b	R/W	0 = Do not include the range configuration register value (default) 1 = Include the range configuration register value Select whether 4-bit input range setting in the SDO-x output bit stream.
D[7:4]	Reserved	0000b	0000b	R	Reserved.
D[3]	PAR_EN	0b	–	R/W	0 = Output data does not contain parity information (default) 1 = Two parity bits (ADC output and output data frame) are appended to the LSBs of the output data It's an even parity, and all output data bits are included.
D[2:0]	DATA_VAL[2:0]	000b	000b	R/W	0xx = Value output is the conversion data 100 = Value output is all 0's 101 = Value output is all 1's 110 = Value output is alternating 0's and 1's 111 = Value output is alternating 00's and 11's These bits control the data value output by the converter.

NOTES:
1. Address for bits [7:0] = 10h. Address for bits [15:8] = 11h. Address for bits [23:16] = 12h. Address for bits [31:24] = 13h.
2. Power-on reset valid.
3. Application reset valid.

REGISTER MAPS (continued)

RANGE_SELECTION Register (Address = 14h)

Table 14. RANGE_SELECTION Register Details

BITS	BIT NAME	POWER-ON RESET (2)	APPLICATION RESET (3)	TYPE	DESCRIPTION
D[31:16]	Reserved	0000h	0000h	R	Reserved.
D[15:8]	Reserved	00h	00h	R	Reserved.
D[7]	Reserved	0b	0b	R	Reserved.
D[6]	INTREF_DIS	0b	0b	R/W	0 = Internal reference is enabled (default) 1 = Internal reference is disabled
D[5:4]	Reserved	00b	00b	R	Reserved.
D[3:0]	RANGE_SEL[3:0]	0000b	--	R/W	0001 = ±2.5 × V_{REF} 0011 = ±1.25 × V_{REF} 0100 = ±0.625 × V_{REF} 1001 = 2.5 × V_{REF} 1011 = 1.25 × V_{REF} These bits comprise the 4-bit register that selects the nine input ranges of the ADC.

NOTES:
1. Address for bits [7:0] = 14h. Address for bits [15:8] = 15h. Address for bits [23:16] = 16h. Address for bits [31:24] = 17h.
2. Power-on reset valid.
3. Application reset valid.

REGISTER MAPS (continued)

ALARM_OUTPUT Register (Address = 20h)

Table 15. ALARM_OUTPUT Register Details

BITS	BIT NAME	POWER-ON RESET (2)	APPLICATION RESET (3)	TYPE	DESCRIPTION
D[31:16]	Reserved	0000h	0000h	R	Reserved.
D[15]	ACTIVE_VDD_L_FLAG	0b	0b	R	Enable ALARM Output Flag for Low AVDD Voltage 0 = No ALARM condition (default) 1 = ALARM VDD low enable
D[14]	ACTIVE_VDD_H_FLAG	0b	0b	R	Enable ALARM Output Flag for High AVDD Voltage 0 = No ALARM condition (default) 1 = ALARM VDD high enable
D[13:12]	Reserved	00b	00b	R	Reserved.
D[11]	ACTIVE_IN_L_FLAG	0b	0b	R	Enable ALARM Output Flag for High Input Voltage 0 = No ALARM condition (default) 1 = ALARM input low enable
D[10]	ACTIVE_IN_H_FLAG	0b	0b	R	Enable ALARM Output Flag for Low Input Voltage 0 = No ALARM condition (default) 1 = ALARM input high enable
D[9:8]	Reserved	00b	00b	R	Reserved.
D[7]	TRP_VDD_L_FLAG	0b	0b	R	Enable Tripped ALARM Output Flag for Low AVDD Voltage 0 = No ALARM condition (default) 1 = ALARM VDD low tripped enable
D[6]	TRP_VDD_H_FLAG	0b	0b	R	Enable Tripped ALARM Output Flag for High AVDD Voltage 0 = No ALARM condition (default) 1 = ALARM VDD high tripped enable
D[5]	TRP_IN_L_FLAG	0b	0b	R	Enable Tripped ALARM Output Flag for High Input Voltage 0 = No ALARM condition (default) 1 = ALARM input high tripped enable
D[4]	TRP_IN_H_FLAG	0b	0b	R	Enable Tripped ALARM Output Flag for Low Input Voltage 0 = No ALARM condition (default) 1 = ALARM input low tripped enable
D[3:1]	Reserved	000b	000b	R	Reserved. Reads return 000b.
D[0]	OVW_ALARM	0b	0b	R	Enable Logical OR Outputs All Tripped ALARM Flags 0 = No ALARM condition (default) 1 = ALARM Logical OR Outputs All Tripped ALARM Flags enable

NOTES:
1. Address for bits [7:0] = 20h. Address for bits [15:8] = 21h. Address for bits [23:16] = 22h. Address for bits [31:24] = 23h.
2. Power-on reset valid.
3. Application reset valid.

REGISTER MAPS (continued)

ALARM_HIGH_THRES Register (Address = 24h)

Table 16. ALARM_HIGH_THRES Register Details

BITS	BIT NAME	POWER-ON RESET (2)	APPLICATION RESET (3)	TYPE	DESCRIPTION
D[31:24]	INP_ALRM_HYST[7:0]	00h	00h	R/W	INP_ALRM_HYST[7:2]: 6-bit hysteresis value for the input ALARM. INP_ALRM_HYST[1:0] must be set to 00b.
D[23:16]	Reserved	00h	00h	R	Reserved.
D[15:0]	INP_ALRM_HIGH_TH[15:0]	FFFFh	FFFFh	R/W	Threshold for input high alarm.

NOTES:
1. Address for bits [7:0] = 24h. Address for bits [15:8] = 25h. Address for bits [23:16] = 26h. Address for bits [31:24] = 27h.
2. Power-on reset valid.
3. Application reset valid.

ALARM_LOW_THRES Register (Address = 28h)

Table 17. ALARM_LOW_THRES Register Details

BITS	BIT NAME	POWER-ON RESET (2)	APPLICATION RESET (3)	TYPE	DESCRIPTION
D[31:16]	Reserved	0000h	0000h	R	Reserved. Reads return 0000h.
D[15:0]	INP_ALRM_LOW_TH[15:0]	0000h	0000h	R/W	Threshold for input low alarm.

NOTES:
1. Address for bits [7:0] = 28h. Address for bits [15:8] = 29h. Address for bits [23:16] = 2Ah. Address for bits [31:24] = 2Bh.
2. Power-on reset valid.
3. Application reset valid.

INPUT_FLOATING_DETECTION_EN Register (Address = 2Ch)

This register controls the input floating detection block enabled or disabled.

Table 18. INPUT_FLOATING_DETECTION_EN Register Details

BITS	BIT NAME	POWER-ON RESET (2)	APPLICATION RESET (3)	TYPE	DESCRIPTION
D[31:1]	Reserved	00000000h	00000000h	R	Reserved. Reads return 00000000h.
D[0]	INP_DETECT_EN	0b	0b	R/W	0 = Input floating detection disabled (default) 1 = Input floating detection enabled

NOTES:
1. Address for bits [7:0] = 2Ch. Address for bits [15:8] = 2Dh. Address for bits [23:16] = 2Eh. Address for bits [31:24] = 2Fh.
2. Power-on reset valid.
3. Application reset valid.

REGISTER MAPS (continued)

INPUT_FLOATING_DETECTION_STATUS Register (Address = 30h)

This register controls the input floating detection block enabled or disabled.

Table 19. INPUT_FLOATING_DETECTION_STATUS Register Details

BITS	BIT NAME	POWER-ON RESET (2)	APPLICATION RESET (3)	TYPE	DESCRIPTION
D[31:1]	Reserved	00000000h	00000000h	R	Reserved. Reads return 00000000h.
D[0]	INP_FLOAT_STS	0b	0b	R	0 = Input is not floating (default) 1 = Input is floating

NOTES:
1. Address for bits [7:0] = 30h. Address for bits [15:8] = 31h. Address for bits [23:16] = 32h. Address for bits [31:24] = 33h.
2. Power-on reset valid.
3. Application reset valid.

REVISION HISTORY

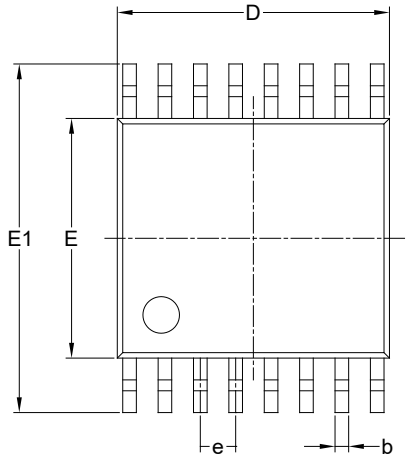
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

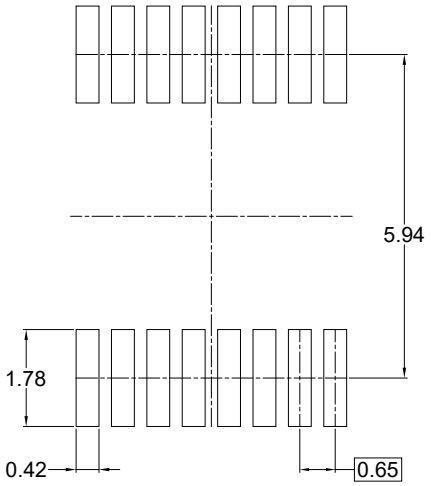
MARCH 2023 – REV.A to REV.A.1	Page
Updated Electrical Characteristics section	7

Changes from Original (DECEMBER 2022) to REV.A	Page
Changed from product preview to production data	All

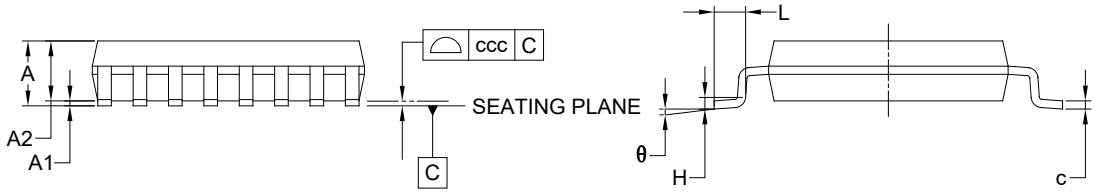
PACKAGE OUTLINE DIMENSIONS

TSSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)

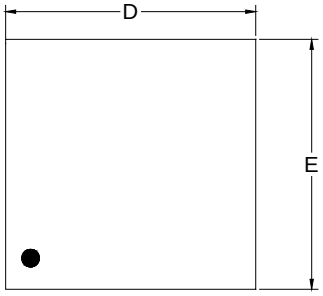


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

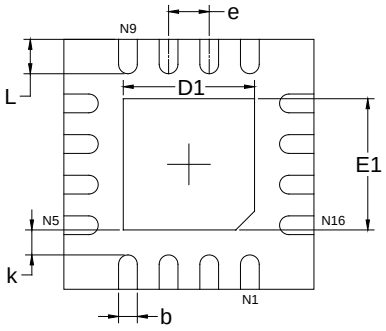
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

PACKAGE OUTLINE DIMENSIONS

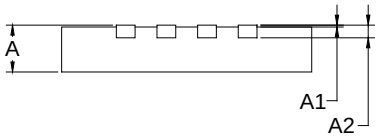
TQFN-4×4-16L



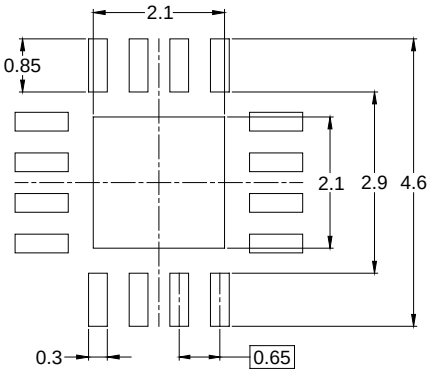
TOP VIEW



BOTTOM VIEW



SIDE VIEW



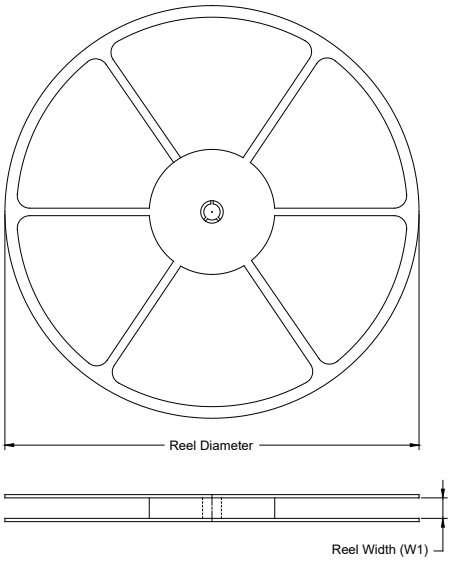
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	3.900	4.100	0.154	0.161
D1	2.000	2.200	0.079	0.087
E	3.900	4.100	0.154	0.161
E1	2.000	2.200	0.079	0.087
k	0.200 MIN		0.008 MIN	
b	0.250	0.350	0.010	0.014
e	0.650 TYP		0.026 TYP	
L	0.450	0.650	0.018	0.026

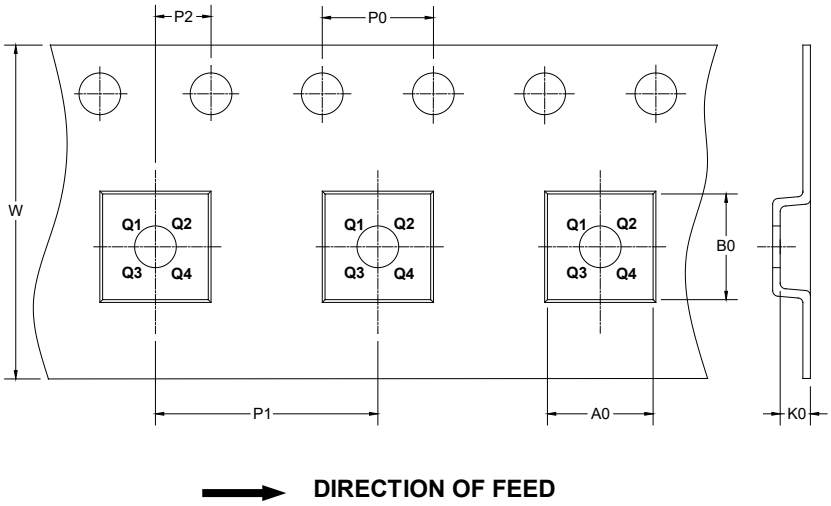
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



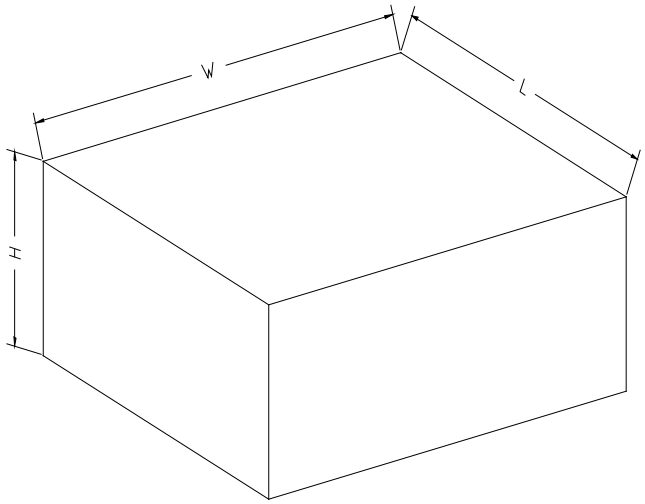
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-16	13″	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1
TQFN-4×4-16L	13″	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002