SGM48524Q
Dual 5A, High-Speed, Low-Side Gate Driver with Negative Input Voltage Capability

GENERAL DESCRIPTION

The SGM48524Q is a dual high-speed low-side gate driver for MOSFET and IGBT power switches. It has rail-to-rail driving capability and can sink and source up to 5A peak current with capacitive loads. The propagation delays are very short and well matched between the two channels that make the device very fit for applications that need accurate dual gate driving such as synchronous rectifiers. The matched propagation delays also allow for paralleling the two channels when higher driving current is required, such as for paralleled switches. The input voltage thresholds are fixed, independent of supply voltage (V_{DD}) and are compatible with low voltage TTL and CMOS logic. Noise immunity is excellent due to the wide hysteresis window between the input low and high thresholds. The device has internal pull-up/pull-down resistors on the input pins to ensure low state on the driver output when the inputs are floating.

The SGM48524Q is a dual non-inverting driver. It has independent enable pins (ENA and ENB) for each channel with active-high logic that can be left open for normal operation because of internal pull-up to VDD.

The SGM48524Q is available in a Green SOIC-8 package. It operates over a temperature range of -40℃ to +125℃.

This device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  - **Device Temperature Grade 1**
  - **T_A = -40℃ to +125℃**
- **Two Independent Gate Drive Channels**
- **4.5V to 18V Single Supply Range (V_{DD})**
- **5A Peak Source/Sink Pulse Current Drive**
- **Independent Enable Pin for Each Channel**
- **TTL and CMOS Compatible Logic Threshold**
- **Logic Levels Independent of Supply Voltage**
- **Hysteretic Input Logic for High Noise Immunity**
- **Outputs are Logic Low when Inputs are Floating**
- **Negative Voltage Handling Capability:**
  - **-8V DC at Inputs**
  - **-2V, 200ns Pulse for Outputs (OUTx)**
- **Glitch-Free Operation at Power-Up and Power-Down: Outputs Pulled Low during Supply UVLO**
- **Fast Propagation Delays: 18ns (TYP)**
- **Fast Rise Time: 7ns (TYP)**
- **Fast Fall Time: 8ns (TYP)**
- **Delay Matching between Two Channels: 1ns (TYP)**
- **Channels can be Paralleled for Higher Drive Current**
- **Available in a Green SOIC-8 Package**

APPLICATIONS

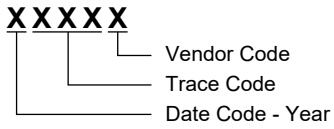
Power MOSFETs
IGBT Driving for Power Supplies
DC/DC Converters
Solar Power, Motor Drivers
Gate Drive for Emerging Wide Bandgap Devices

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE TOP MARKING	PACKING OPTION
SGM48524Q	SOIC-8	-40℃ to +125℃	SGM48524QS8G/TR	SGM 009S8 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} ..... -0.3V to 20V
INA, INB, ENA, ENB Voltage ..... -8V to 20V
OUTA, OUTB Voltage (DC) ..... -0.3V to V_{DD} + 0.3V
OUTA, OUTB Voltage (Pulse < 200ns) ..... -2V to V_{DD} + 0.3V
Maximum Output Pulsed Source/Sink Current (0.5μs), I_{OUT_PULSED} 5A
Package Thermal Resistance
SOIC-8, θ_{JA} ..... 120℃/W
SOIC-8, θ_{JC} ..... 54℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 4.5V to 18V
Input Voltage, INA, INB ..... -2V to 18V
Enable Voltage, ENA and ENB ..... -2V to 18V
Operating Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

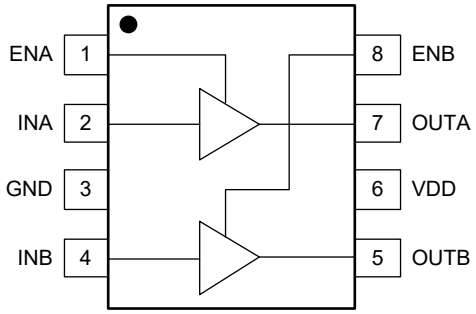
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



SOIC-8

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	ENA	I	Channel A Enable Input. Pull ENA high or leave it floating to enable OUTA output. Pull ENA low to disable OUTA output, ignoring INA state.
2	INA	I	Channel A Non-Inverting Input. OUTA is logic low if INA is unbiased or left floating.
3	GND	—	Ground. Reference pin for all signals.
4	INB	I	Channel B Non-Inverting Input. OUTB is logic low if INB is unbiased or left floating.
5	OUTB	O	Channel B Output.
6	VDD	I	Power Supply Input.
7	OUTA	O	Channel A Output.
8	ENB	I	Channel B Enable Input. Pull ENB high or leave it floating to enable OUTB output. Pull ENB low to disable OUTB output, ignoring INB state.

NOTE: I: Input; O: Output.

FUNCTION TABLE

ENA	ENB	INA	INB	OUTA	OUTB
H	H	L	L	L	L
H	H	L	H	L	H
H	H	H	L	H	L
H	H	H	H	H	H
L	L	Any	Any	L	L
Any	Any	Floating	Floating	L	L
Floating	Floating	L	L	L	L
Floating	Floating	L	H	L	H
Floating	Floating	H	L	H	L
Floating	Floating	H	H	H	H

TYPICAL APPLICATION

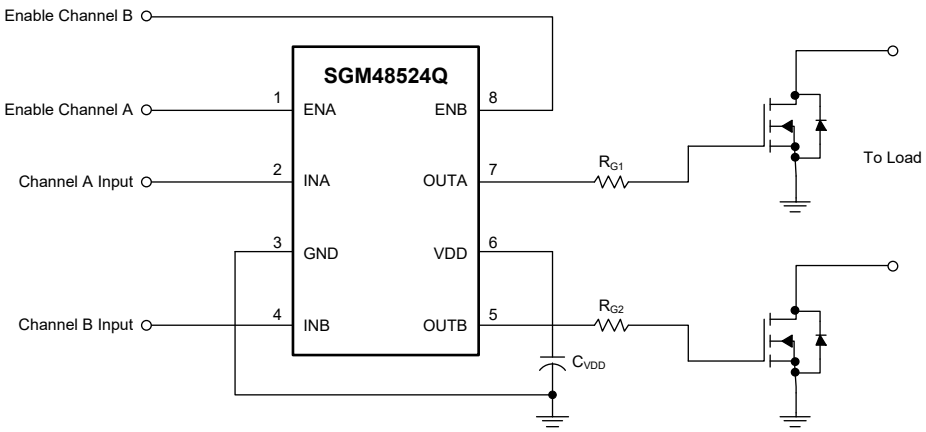


Figure 1. SGM48524Q Typical Application

ELECTRICAL CHARACTERISTICS

(V_{DD} = 12V, C_{VDD} = 1μF, T_A = T_J = -40℃ to +125℃, typical values are at T_A = +25℃. Currents are positive into and negative out of the specified terminal, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supplies						
VDD Supply Voltage	V_{DD}		4.5		18	V
VDD Start-Up Current	I_{DD_OFF}	V_{DD} = 3.4V, V_{INA} = V_{INB} = 0V		38	65	μA
		V_{DD} = 3.4V, V_{INA} = V_{INB} = V_{DD}		58	91	
Supply Start Threshold	V_{ON}	T_A = +25℃	3.8	4.2	4.5	V
		T_A = -40℃ to +125℃	3.7	4.2	4.7	
Minimum Operating VDD Voltage after Supply is Started	V_{OFF}		3.4	3.85	4.3	V
VDD Supply Voltage Hysteresis	V_{DD_HYS}		0.2	0.35	0.5	V
Input Pins (INA, INB)						
Input Signal High Threshold	V_{IN_H}	Output high for non-inverting input pins	1.8	2.0	2.2	V
Input Signal Low Threshold	V_{IN_L}	Output low for non-inverting input pins	1.0	1.2	1.4	V
Input Hysteresis	V_{IN_HYS}		0.6	0.8	1.0	V
Enable Pins (ENA, ENB)						
Enable Signal High Threshold	V_{EN_H}	Output enabled	1.8	2.0	2.2	V
Enable Signal Low Threshold	V_{EN_L}	Output disabled	1.0	1.2	1.4	V
Enable Hysteresis	V_{EN_HYS}		0.6	0.8	1.0	V
Output Pins (OUTA, OUTB)						
High Level Output Voltage	V_{OH}	V_{OH} = V_{DD} - V_{OUT}, I_{OUT} = -10mA			0.058	V
Low Level Output Voltage	V_{OL}	I_{OUT} = 10mA			0.009	V
Output Pull-Up Resistance (1)	R_{OH}	I_{OUT} = -10mA		3.7	5.8	Ω
Output Pull-Down Resistance	R_{OL}	I_{OUT} = 10mA		0.55	0.9	Ω
Peak Output Current	I_{PK_SOURCE}	C_L = 0.22μF, f_{SW} = 1kHz		5		A
	I_{PK_SINK}			5		A
Protection Circuits						
Thermal Shutdown Temperature	T_{TSD}			165		℃
Thermal Shutdown Temperature Hysteresis	T_{HYS}			15		℃

NOTE:
1. R_{OH} represents constant pull-up resistance only.

SWITCHING CHARACTERISTICS

(V_{DD} = 12V, C_{VDD} = 1μF, T_A = T_J = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time (1)	t_R	C_L = 1.8nF		7		ns
Fall Time (1)	t_F	C_L = 1.8nF		8		ns
Delay Matching Between 2 Channels	t_M	INA = INB, OUTA and OUTB at 50% transition point		1		ns
Minimum Input Pulse Width that Changes the Output State	t_{PW}			15		ns
Input to Output Propagation Delay (1)	t_{D1}	C_L = 1.8nF, 5V input pulse		11		ns
	t_{D2}	C_L = 1.8nF, 5V input pulse		18		
EN to Output Propagation Delay (1)	t_{D3}	C_L = 1.8nF, 5V enable pulse		11		ns
	t_{D4}	C_L = 1.8nF, 5V enable pulse		18		

NOTE:
1. See timing diagrams in Figure 2 and Figure 3.

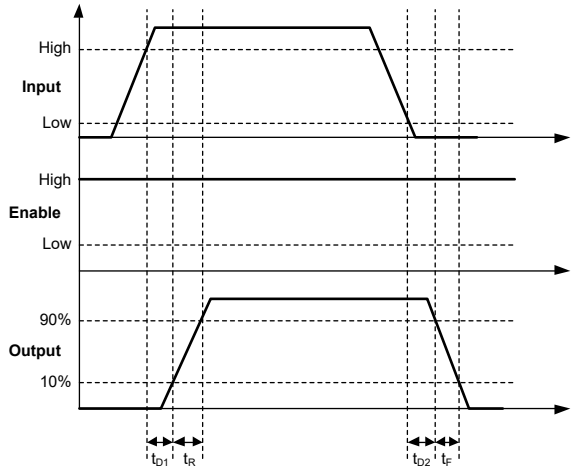


Figure 2. Non-Inverting Input Driver Operation

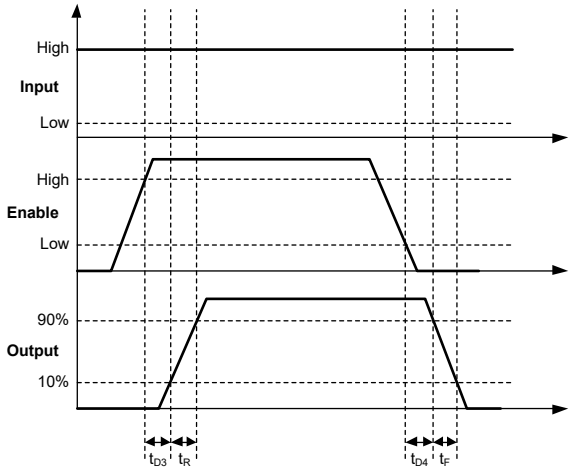
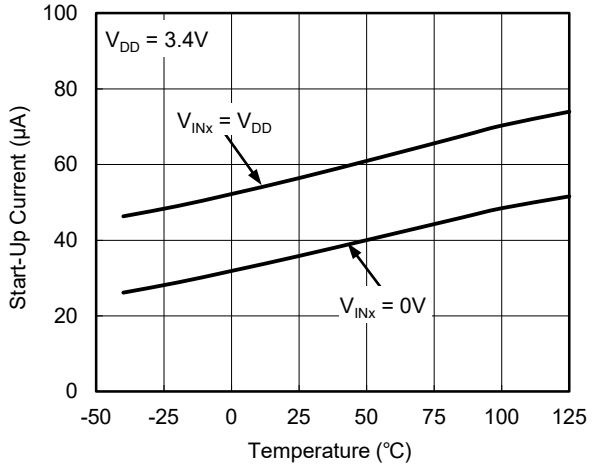


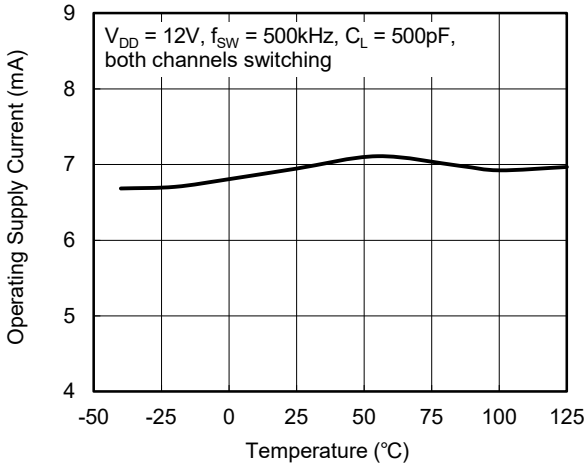
Figure 3. Enable Function (For Non-Inverting Input Driver Operation)

TYPICAL PERFORMANCE CHARACTERISTICS

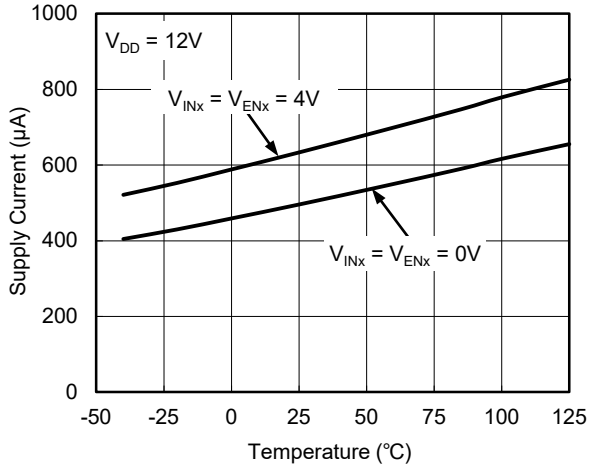
Start-Up Current vs. Temperature



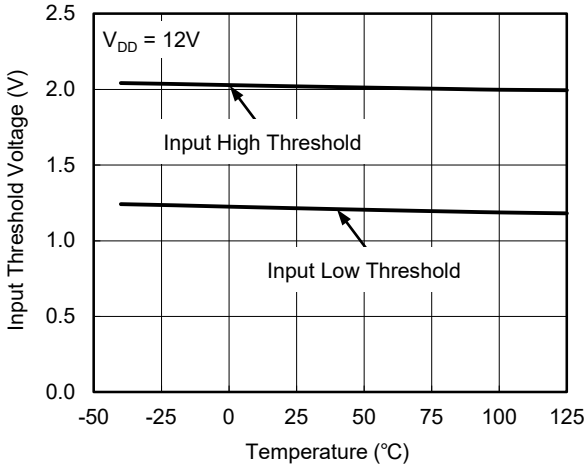
Operating Supply Current vs. Temperature (Outputs Switching)



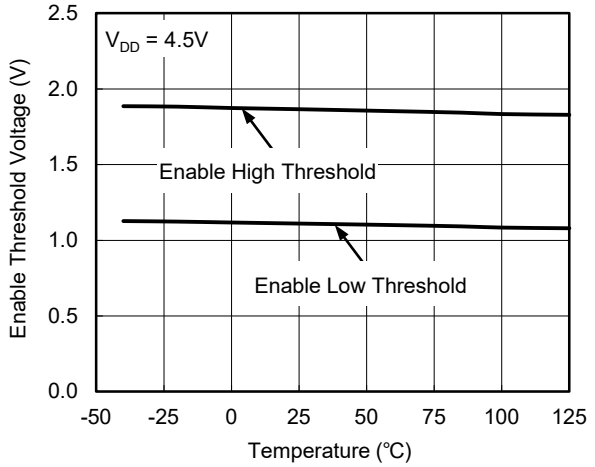
Supply Current vs. Temperature (Outputs in DC On/Off Condition)



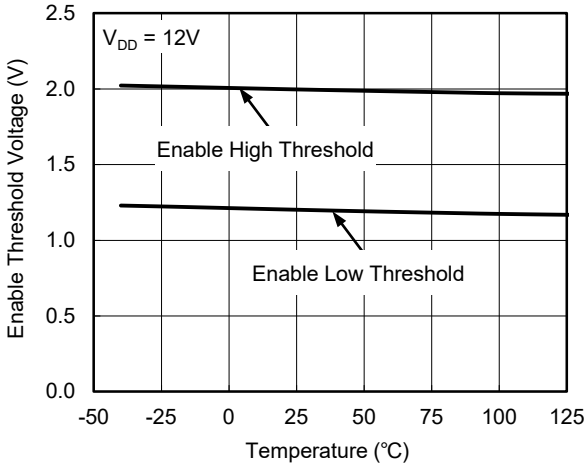
Input Threshold Voltage vs. Temperature



Enable Threshold Voltage vs. Temperature

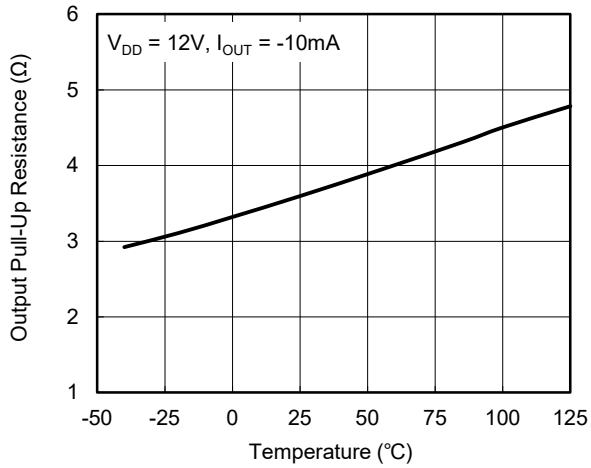


Enable Threshold Voltage vs. Temperature

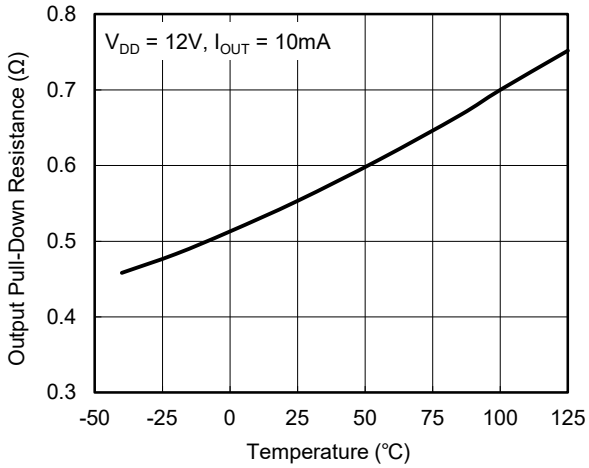


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

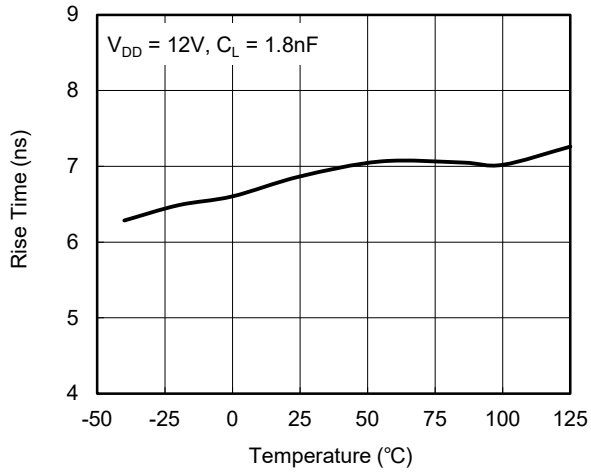
Output Pull-Up Resistance vs. Temperature



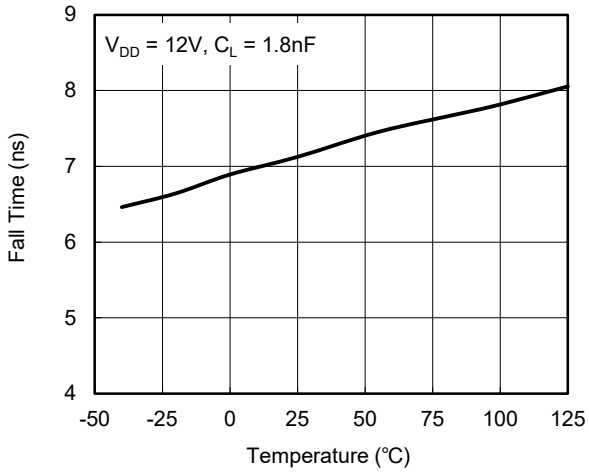
Output Pull-Down Resistance vs. Temperature



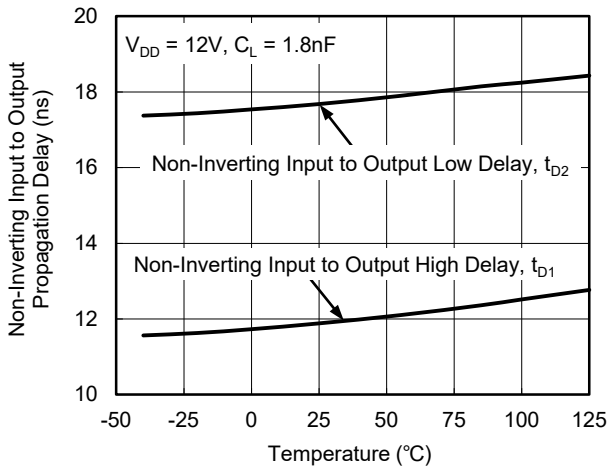
Rise Time vs. Temperature



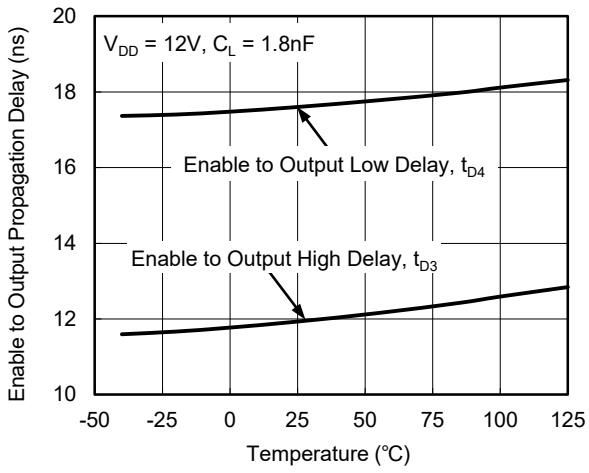
Fall Time vs. Temperature



Non-Inverting Input to Output Propagation Delay vs. Temperature

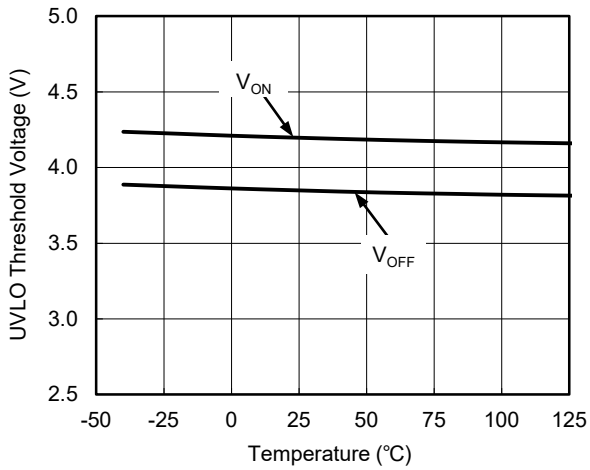


Enable to Output Propagation Delay vs. Temperature

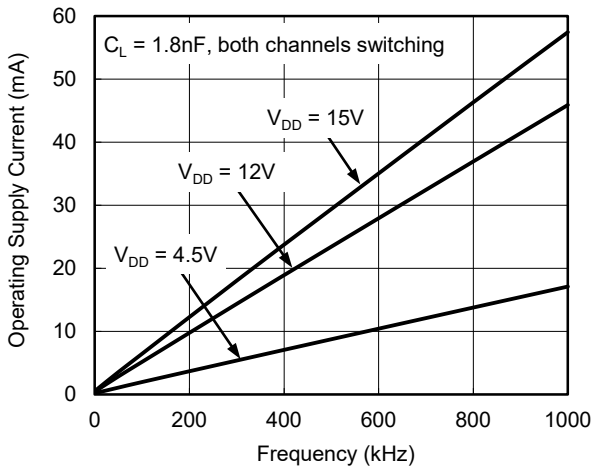


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

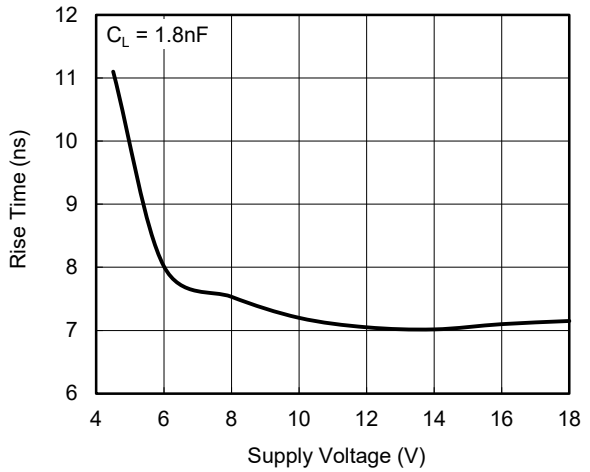
UVLO Threshold Voltage vs. Temperature



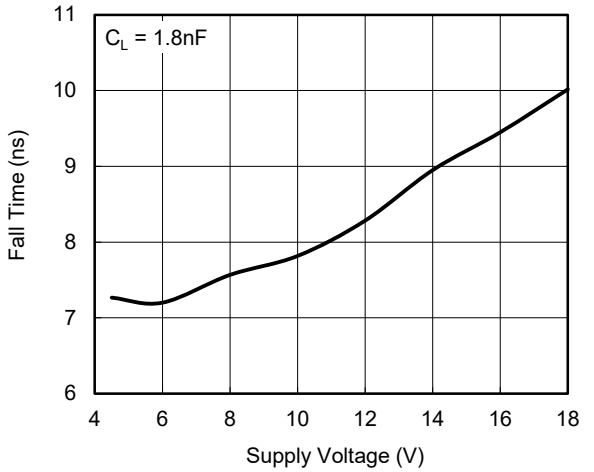
Operating Supply Current vs. Frequency



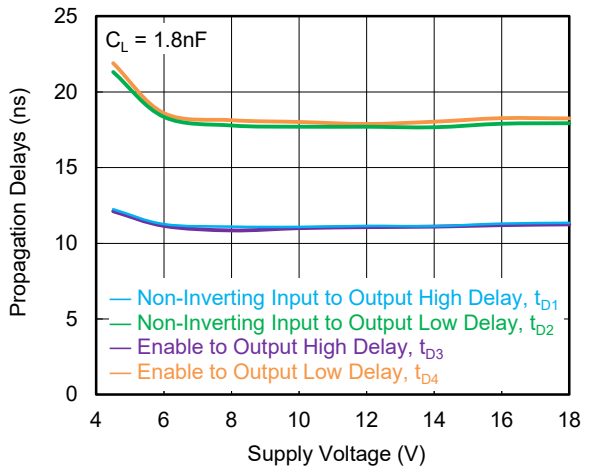
Rise Time vs. Supply Voltage



Fall Time vs. Supply Voltage



Propagation Delays vs. Supply Voltage



FUNCTIONAL BLOCK DIAGRAM

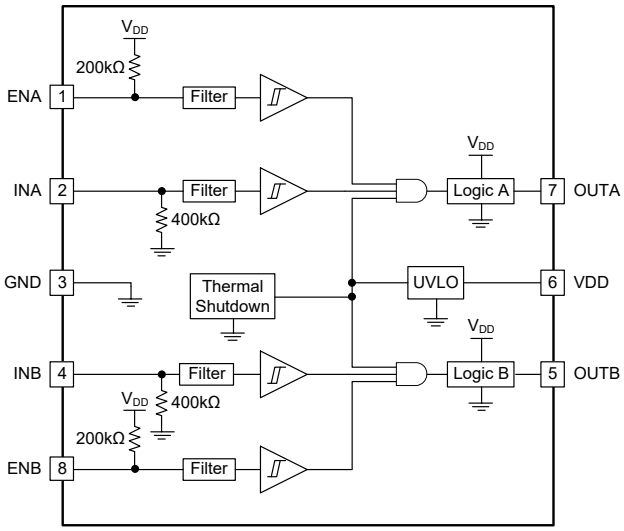


Figure 4. SGM48524Q Block Diagram

DETAILED DESCRIPTION

The SGM48524Q dual-channel, low-side, high-speed gate driver is among the top level devices in the market featuring a 5A source/sink current capability and industry best-in-class switching characteristics. It has several other prominent features as listed in Table 1 assuring that they are reliable and efficient gate driving solutions for power switches in high frequency applications.

Under-Voltage Lockout for VDD

The internal under-voltage lockout (UVLO) protection keeps the outputs in low state when the VDD supply voltage is insufficient for proper operation of the chip. If V_{DD} rises but its voltage does not reach UVLO threshold, the outputs are logic low, ignoring the state of the inputs. The UVLO rising threshold level is 4.2V (TYP) and has a 0.35V (TYP) hysteresis band to prevent output from chattering when V_{DD} has large superimposed noise or other fluctuations. The safe low voltage (less than 5V) operating capability along with the excellent switching characteristics makes the device well suited for driving GaN power switches.

Table 1. Prominent Features and Benefits

FEATURE	BENEFIT
Best-in-class propagation delays (18ns, TYP).	Very low delay and distortion in pulse transmission.
Excellent delay matching between channels (1ns, TYP).	Allows paralleling of the channel outputs for double current driving capability. It is especially useful for driving paralleled power switches.
Wide supply operating range (V_{DD} from 4.5V to 18V).	Design Flexibility.
Wide operating ambient temperature range (-40℃ to +125℃).	Wider system operating temperature range and smaller cooling system.
UVLO protection on VDD.	Driver outputs are logic low in UVLO condition to ensure controlled and glitch-free driving during power-up and power-down.
Outputs are logic low when inputs (INx) are floating.	This safety feature prevents unexpected gate pulses during abnormal situations such as the conditions tested in the safety certification.
Outputs are enabled when enable inputs (ENx) are floating.	This feature provides pin-to-pin compatibility with other similar products in those designs where pin 1 and 8 are floating.
Wide hysteresis CMOS/TTL compatible input and enable thresholds.	Improved noise immunity while compatible with digital logic (3.3V, 5V).
Input/enable pins voltage levels are not restricted by $V_{DD.}$	Simplified system especially in the auxiliary bias supply architecture.
Ability to handle -8V V_{DC} (MAX) at input pins.	Increased robustness in noisy environments.

DETAILED DESCRIPTION (continued)

If the enable pin is active or floating during power-up, the SGM48524Q output remains low until V_{DD} exceeds the UVLO threshold. Then the output is controlled by the input signal with a magnitude that follows V_{DD} (see Figure 5 for a non-inverting channel).

Because VDD pin is the supply source for the device internal circuits, it is recommended to use two V_{DD} surface mount bypass capacitors to prevent noise problems caused by high speed switching. A small 100nF ceramic capacitor must be soldered as close between the VDD and GND pins as possible. In addition, a larger low ESR capacitor (a few μF) must be placed in parallel and close to the same pins for delivery of the high peak driving currents with sharp rise time. The low impedance characteristic provided by these capacitors allows high frequency and high current driving of the outputs. Avoid using vias for connecting bypass capacitors to the device pins.

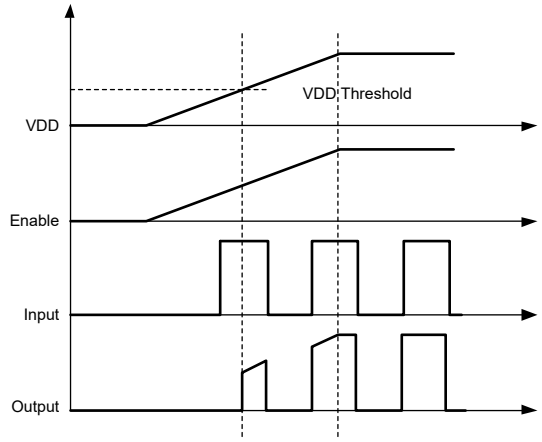


Figure 5. Power-up in a Non-Inverting Driver Channel

Operating Supply Current

The SGM48524Q consumes a very low quiescent I_{DD} current. The lowest quiescent I_{DD} value is reached when the device is fully powered (not in UVLO), and the outputs are in a low or high DC static state and the internal pull-up inputs (enable inputs) are in high or float state. During normal operation, the total I_{DD} current is the sum of three components: the quiescent current, the average I_{OUT} current due to switching and the internal pull-up resistor currents (on enable inputs). Usually the main portion of the supply current is for driving the outputs and the other two can be ignored. For driving MOSFETs with a frequency of f_{SW} and gate charge of Q_g, the average driver output current is $I_{OUT} = Q_g \times f_{SW}$.

Input Stage

SGM48524Q input pins are compatible with TTL and CMOS logic thresholds and are independent of the supply voltage (V_{DD}). The logic high threshold for the SGM48524Q is typically around 2V and the low threshold is around 1.2V. Therefore the inputs can be easily driven by a 3.3V or 5V digital controller. The noise immunity is enhanced due to the relatively wide hysteresis band (2V - 1.2V = 0.8V, TYP) compared to the traditional TTL logic in which the hysteresis is typically less than 0.5V. The input voltage thresholds in the SGM48524Q are tightly controlled to simplify the system design and assure stable operation against wide temperature variations. Also the device is designed with very low parasitic input pin capacitances to allow high speed switching.

An important safety feature of the driver is that if any of the input pins floats, the corresponding channel output will be held in the low state. This feature is implemented by the GND pull-down resistors on the non-inverting inputs as shown in Figure 4.

The input driving signal must have short rise or fall time. This condition is normally satisfied when the input signals are generated by a PWM controller or logic gate (with transition times < 200ns). If the input transition is too slow, the output may chatter several times (at high frequency) before going to its new stable state. The wide input hysteresis of the device minimizes the concern for such problem even for other logic thresholds. However, the designer should make sure the implementation satisfies the driver input requirements. To limit the rise or fall time of the gate pulse on the output, it is recommended to use an external series resistance between the driver output and the gate of the power device. This resistor reduces the switching gate charge losses in the driver output stage because a portion of the loss will dissipate in the resistor.

DETAILED DESCRIPTION (continued)

Enable

The enable function is very useful in some applications that need to block gate pulses depending on the system operating conditions. For example, in a synchronous rectifier and in light load conditions, it may be necessary to disable gate signal to avoid negative current in the device for improving efficiency or to prevent boosting in a Buck converter.

This driver has an independent active-high enable pin (ENx). Similar to the driver inputs, the enable pins are independent of the supply voltage with tightly controlled thresholds and are compatible with TTL or CMOS logic. They can be directly controlled by the popular 3.3V and 5V microcontrollers. The ENx pins (x = A or B) are internally pulled up to VDD by pull-up resistors and the output channel x is enabled if ENx input is floating. Therefore the SGM48524Q is pin-to-pin compatible with SGMICRO's previous gate driver. Note that if two channels in a device are paralleled, the enable signals should also be tied together.

Tightly Matched and Low Propagation Delays

The SGM48524Q driver offers very low propagation delay (18ns, TYP) and pulse transmission distortion between input and output. Such low distortion is important in the industry for high frequency switching applications, for example in the synchronous rectifier applications where both SR MOSFETs are driven with one driver. Moreover, the delays between the two channels are extremely well matched with 1ns (TYP) difference. This feature is critically important when accurate timing between dual gate drives is required. For example, in some PFC applications, two paralleled MOSFETs may be need to be driven independently using each output channel and with the same input pulses. The matching gate drivers ensure that they are driven simultaneously with the minimum turn-on or turn-off delay differences. The tight matching also allows for paralleling the two channels to increase current driving capability. The INA and INB pins are tied together as input, and OUTA and OUTB pins are tied together as output. Caution must be exercised that any delay between triggering of the two channels can lead to a shoot-through between outputs. Note that as described in Figure 6, the input signals must also be well matched and with fast rise or fall time. Due to the small differences between the input thresholds, a pulse with slow rise or fall time may add extra delay between signals and even though the maximum propagation mismatch between channels is 4ns the actual mismatch would be much higher. Therefore it is recommended that when inputs are paralleled, only very fast input pulses (20V/μs or greater) are used. Also, the tie point for inputs must be as close as possible to the chip. If possible, adding external series gate resistors between the outputs will also help. Considering small 0Ω series output resistors in the layout is recommended to allow future adjustment in the design if needed.

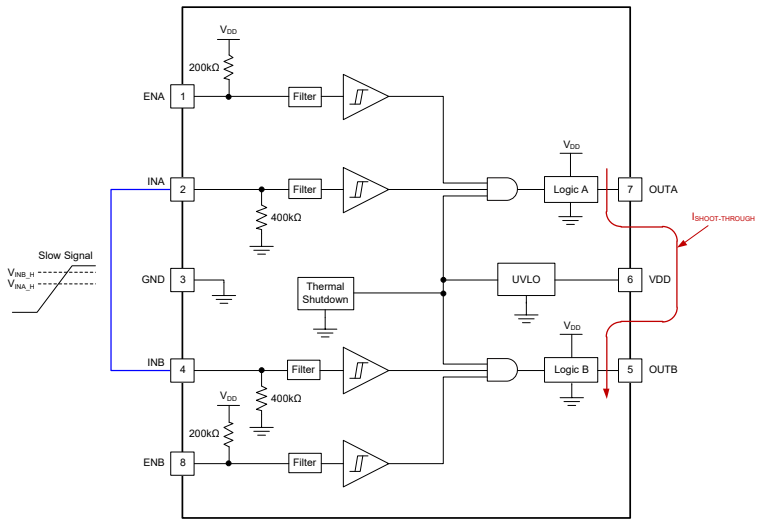


Figure 6. When channels are paralleled for higher drive current, slow rise or fall time of the input pulse can cause shoot-through between device outputs. Inputs with dv/dt higher than 20V/μs are recommended

APPLICATION INFORMATION

In order to achieve fast switching and to reduce losses in the power switches, high current gate drivers with sufficient drive voltage are required. Such function cannot be directly provided by logic controllers usually operating at low power and low voltages such as 3.3V. Even traditional buffer drivers like totem-pole NPN/PNP configurations are not useful as they are not capable for voltage level shifting. A gate driver device provides other advantages in the system such as reduction of the high frequency noise by placing the high current driver close to the power switch, and reduction of power dissipation and thermal stress in controllers because gate-charge power losses are handled by the driver. Moreover, with the emerging of wide band-gap power devices such as GaN based switches that are capable for operating at very high frequency, new gate driving requirements are imposed on the driver devices. Such requirements include operating at low supply voltages (5V or less), low propagation delays and excellent delay matching, and compact layout with low inductance and enhanced thermal capability.

In summary, gate driver devices simplify the system design and provide better performance, lower cost, lower component count and require less space on the board.

Supply Voltage V_{DD}

The supply voltage is selected based on the power switch and driving requirements. Some power switches, need positive gate voltage for turn-on and negative for turn-off and for some other types, it is reversed. In both cases the differential drive voltage is equal to V_{DD} that can be selected in a wide range from 4.5V to 18V. This gate driver can be used for driving of a variety of power switches. Typically for Si MOSFETs, the driving V_{GS} is chosen to be 4.5V, 10V or 12V depending on the application and switch class. For IGBTs a V_{GE} of 15V or 18V is commonly used.

Propagation Delay

The propagation delays depend on the operating switching frequency and the permissible pulse distortion. The SGM48524Q presents very short 18ns (TYP) propagation delays. Switching characteristics with more details are provided to illustrate the propagation and switching performance.

Drive Current and Power Dissipation

MOSFETs are widely used as power switches in many high frequency applications. The SGM48524Q can source and sink 5A at 12V for a pulse width of several hundred nanoseconds for driving MOSFETs. High peak driving current is usually needed for a quick turn on and usually the same amount of current in opposite direction is also needed for switch turn off. The sourcing and sinking actions repeat at the switching frequency and for each transition some energy is dissipated in the driver device.

The amount of power dissipation in the device depends on the following:

- Switching frequency.
- Gate charge required to turn the MOSFET on or off.
- Size of the external gate resistors used (if any).

Gate charge is usually a function of the V_{GS} drive voltage. The drive voltage is $V_{GS} \approx V_{DD}$ (the dropout of the driver, V_{OH}, is normally very low). Note that due to the low quiescent current and the internal bias power, the loss in the driver is effectively equal to the output driving losses caused by drive currents.

Using a discrete capacitor (C_g) as a similar switch gate load for testing, the loss in the driver can be easily estimated. The energy that is needed to charge the capacitor to the supply voltage V_{DD} is given by (1):

$$E_G = \frac{1}{2} C_g V_{DD}^2 \quad (1)$$

It can be proved that the same amount of energy is dissipated in the driver output stage resistances. Also, the same amount of energy is dissipated when the capacitor is discharged by the driver. Therefore, with a switching frequency of f_{SW}, the total power loss (in one channel) is:

$$P_G = C_g V_{DD}^2 f_{SW} \quad (2)$$

As an example, with V_{DD} = 12V, C_g = 10nF and f_{SW} = 200kHz the driver loss is calculated as:

$$P_G = 10nF \times 12V \times 12V \times 200kHz = 288mW \quad (3)$$

APPLICATION INFORMATION (continued)

The test is implemented on MOSFETs to find the equivalent gate capacitance to determine the gate charge required for switching the device. The gate charge includes the impact of the input gate-source and drain-gate capacitances. The drain-gate capacitance also needs current for charge and discharge due to the voltage swing of the drain voltage when the power device is turning on and off. Usually the typical gate charge and maximum gate charge (Q_g) are provided by manufacturers for switching the device under specified conditions. Because $Q_g = C_g V_{DD}$, the power loss in the driver can be calculated from (4) too:

$$P_G = C_g V_{DD}^2 f_{SW} = Q_g V_{DD} f_{SW} \quad (4)$$

For example, for driving a power MOSFET with 50nC of gate charge (Q_g = 50nC) at 500kHz with V_{DD} = 12V, the driver loss due to gate charge will be 0.3W. For this driver that includes two channels, the total loss related to gate charge is doubled when driving similar MOSFETs:

$$P_G = 2 \times 50nC \times 12V \times 0.5MHz = 0.6W \quad (5)$$

When an external series gate resistor, R_g, is used for MOSFET or IGBT, a portion the P_G loss will dissipate on R_g and not inside the driver. With a simplified analysis, the gate driving loss inside each channel can be calculated by (6):

$$P_G = 0.5 \times Q_g \times V_{DD} \times f_{SW} \times \left(\frac{R_{OFF}}{R_{OFF} + R_g} + \frac{R_{ON}}{R_{ON} + R_g} \right) \quad (6)$$

Where $R_{OFF} = R_{OL}$ is the effective pull-down resistance from the channel output to the ground and R_{ON} is the effective resistance of the internal pull-up structure to VDD (in the SGM48524Q).

To find the total loss in the device, the quiescent current losses ($P_Q = I_{DD,Q} \times V_{DD}$) should be added. Due to small quiescent current ($I_{DD,Q} \leq 0.6mA$) of the device, this loss is small and can be ignored. With V_{DD} = 12V, the quiescent loss is P_Q = 0.6mA ×12V = 7.2mW.

The actual driver supply current can be calculated as:

$$I_{DD} \approx \frac{P_G}{V_{DD}} \quad (7)$$

With P_G = 0.6W and V_{DD} = 12V the device supply current will be I_{DD} = 50mA.

Power Supply Recommendations

The operating supply voltage range (V_{DD}) for SGM48524Q gate driver is between 4.5V and 18V. The absolute maximum stress that the device tolerates is 20V. Considering a 2V margin for transient spikes, the maximum range is set to 18V. The minimum limit is dictated by the UVLO protection. In UVLO condition, the outputs are logic low, ignoring the input states. UVLO has an almost 0.35V hysteresis and an operating driver will not shut down unless V_{DD} falls below V_{OFF} = 3.85V (TYP). Therefore, it is important to make sure that for the designed system, the supply ripple or voltage drops do not fall below UVLO lower threshold that triggers device shutdown. A 100nF low ESR ceramic capacitor with another surface-mount capacitor of few microfarads between VDD and GND are necessary to prevent V_{DD} transient drops. Similarly, at start-up, the device starts operation when the VDD pin voltage exceeds the V_{ON} threshold (4.2V, TYP).

REVISION HISTORY

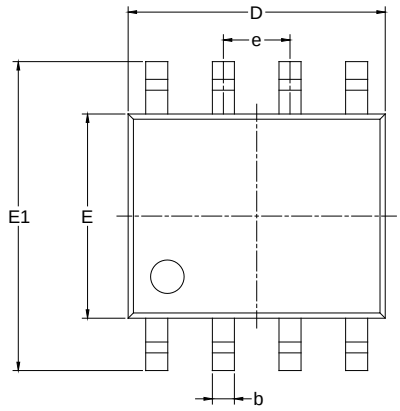
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

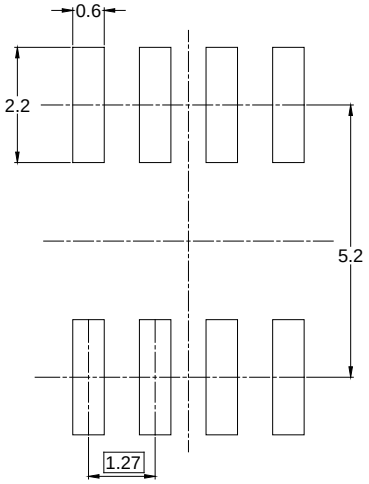
MAY 2023 – REV.A to REV.A.1	Page
Added Absolute Maximum Ratings section	2

Changes from Original (DECEMBER 2022) to REV.A	Page
Changed from product preview to production data	All

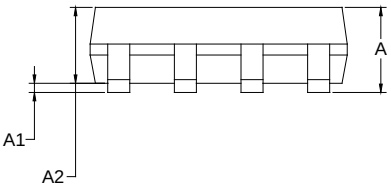
PACKAGE OUTLINE DIMENSIONS

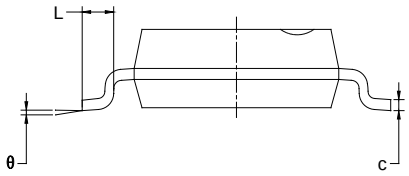
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)



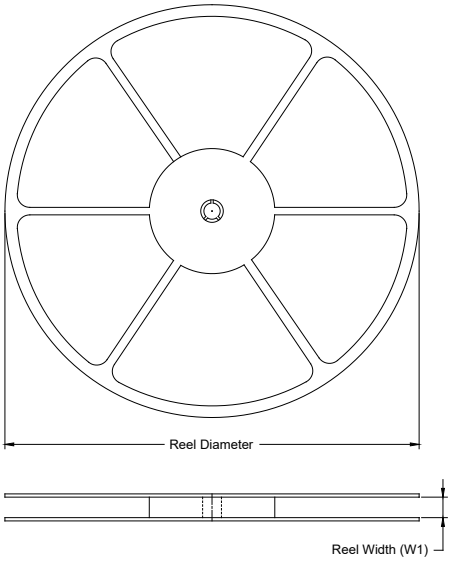


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

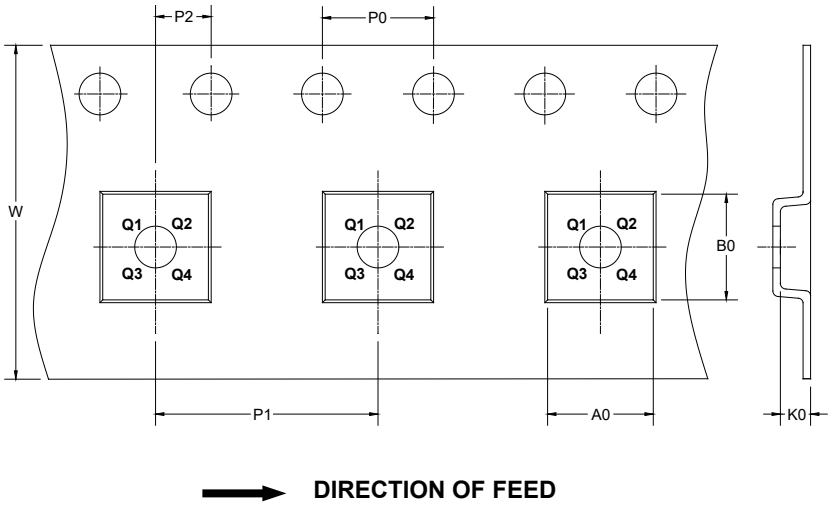
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



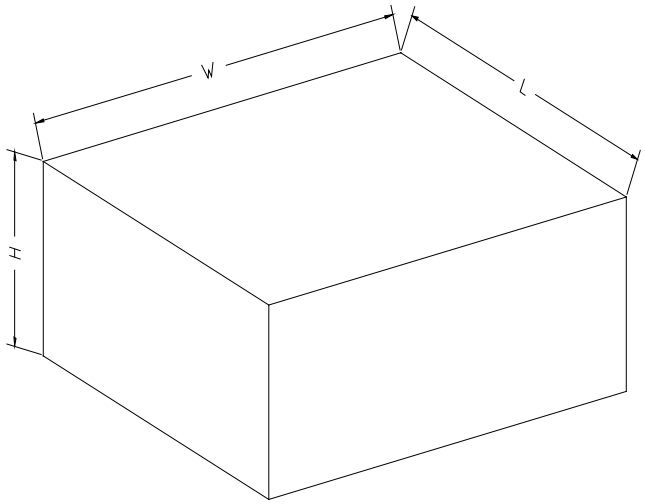
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002